

**Revision : 2.11**

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25	ALC892R

[illegible]

**Model Name:GA-890GPA-UD3H**

## Component value change history


**Version: 2.11**

**P-Code: U98137-0**

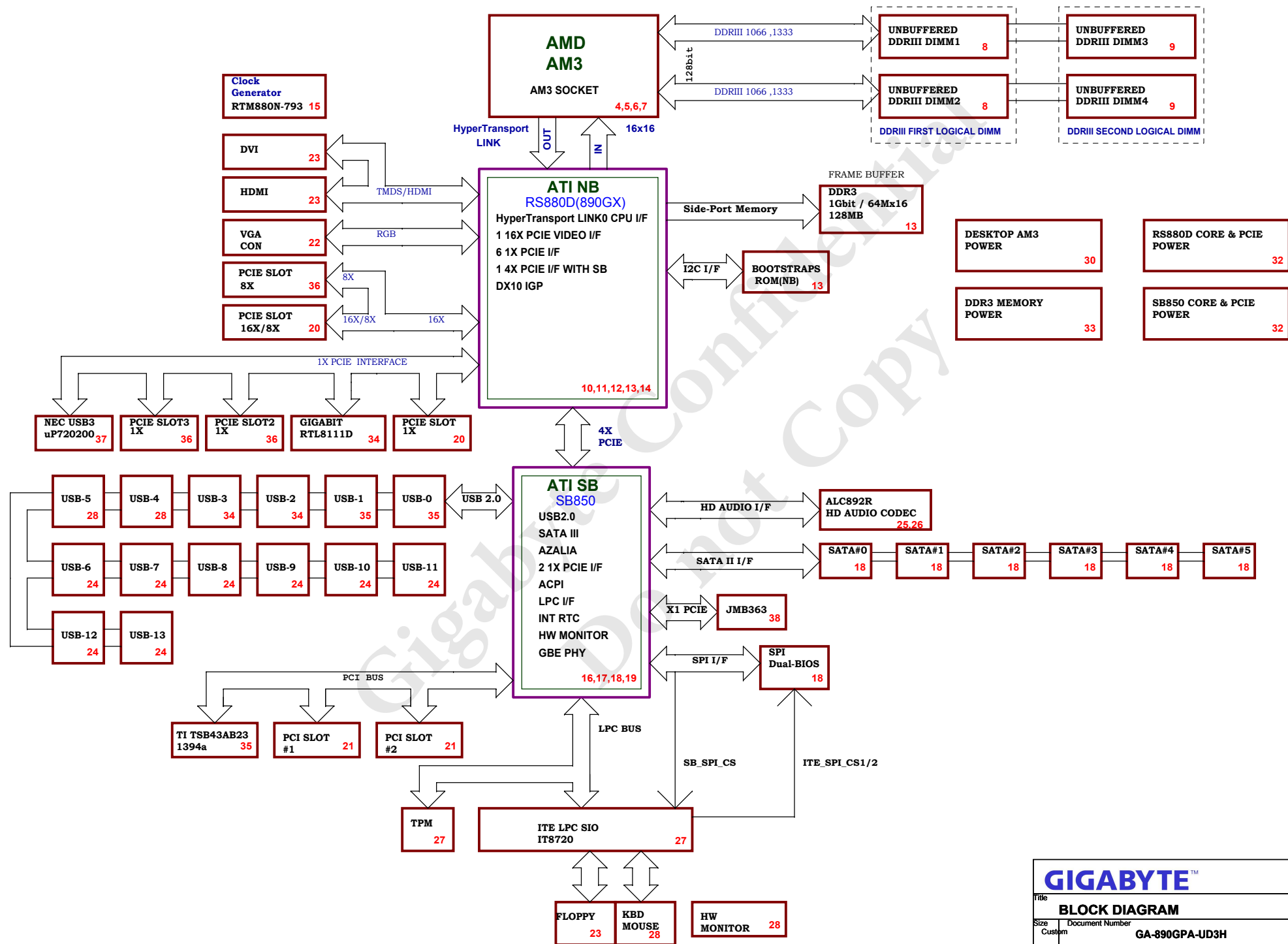
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### Circuit or PCB layout change for next version

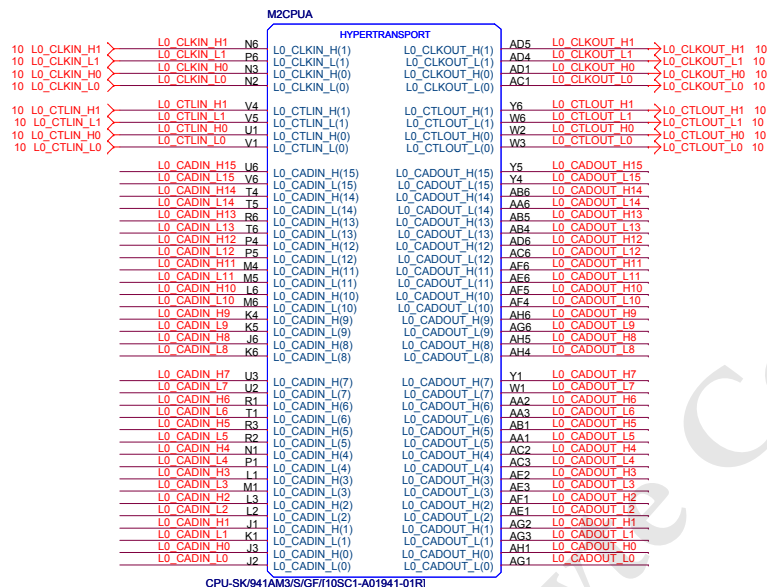
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Title			
<b>BOM &amp; PCB HISTORY</b>			
Size	Document Number		Rev
Custom	<b>GA-890GPA-UD3H</b>		<b>2.11</b>
Date:	Tuesday, June 15, 2010	Sheet	2 of 38

# RS880 CUSTOMER DESKTOP REFERENCE DESIGN



L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] 10  
L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] 10  
L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] 10  
L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] 10



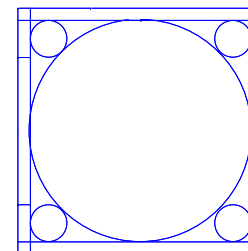
CPU-SK941AM3S/GF[10SC1-A01941-01R]

CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR15V  
CPU\_VDDR = CPU\_VDDR12

VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B

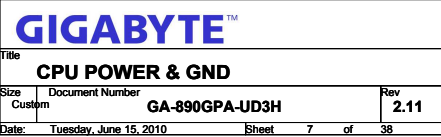
M2CPU

AM2RM/PP/BU/PB[12KRC-04K812-12R]

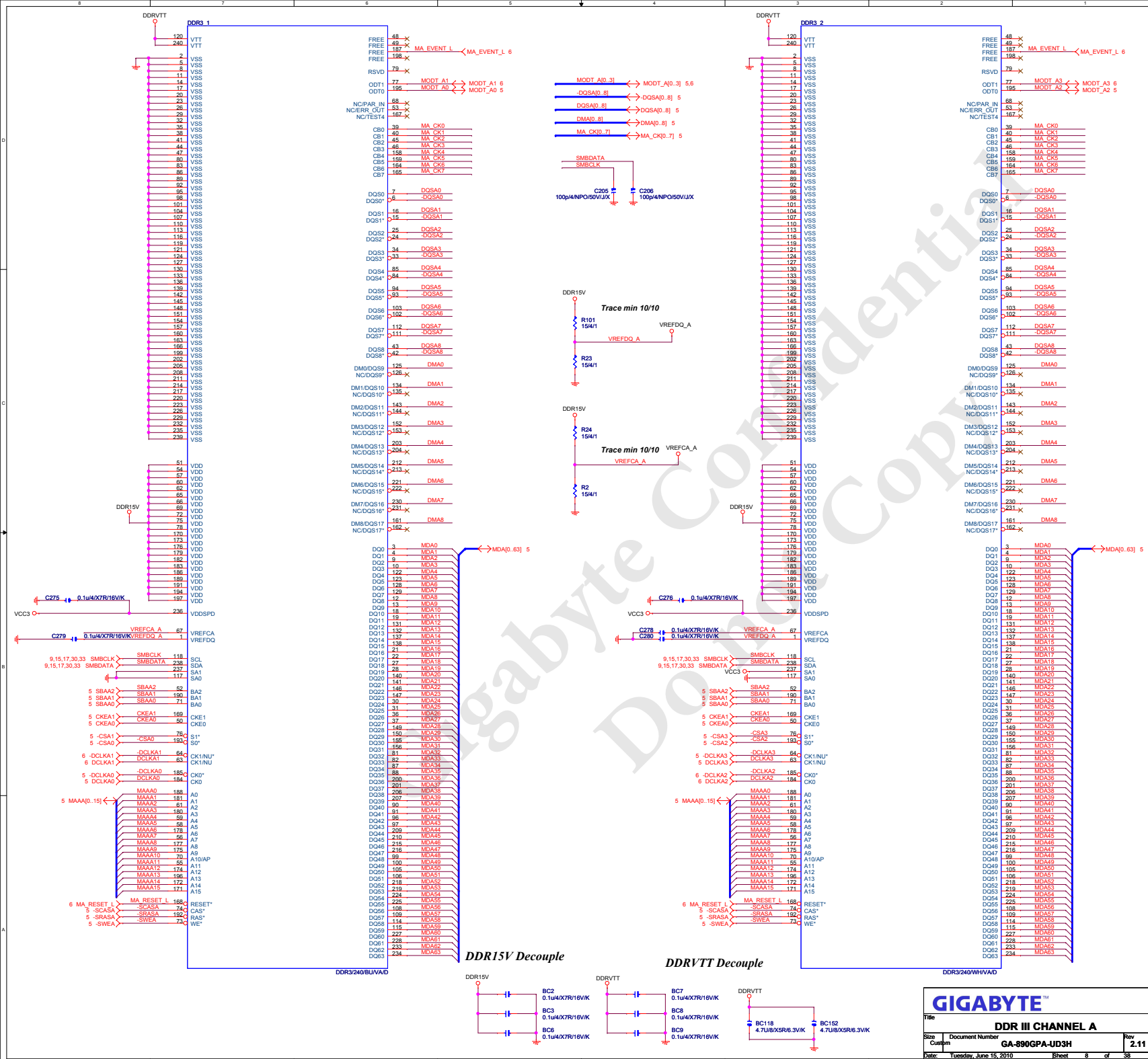




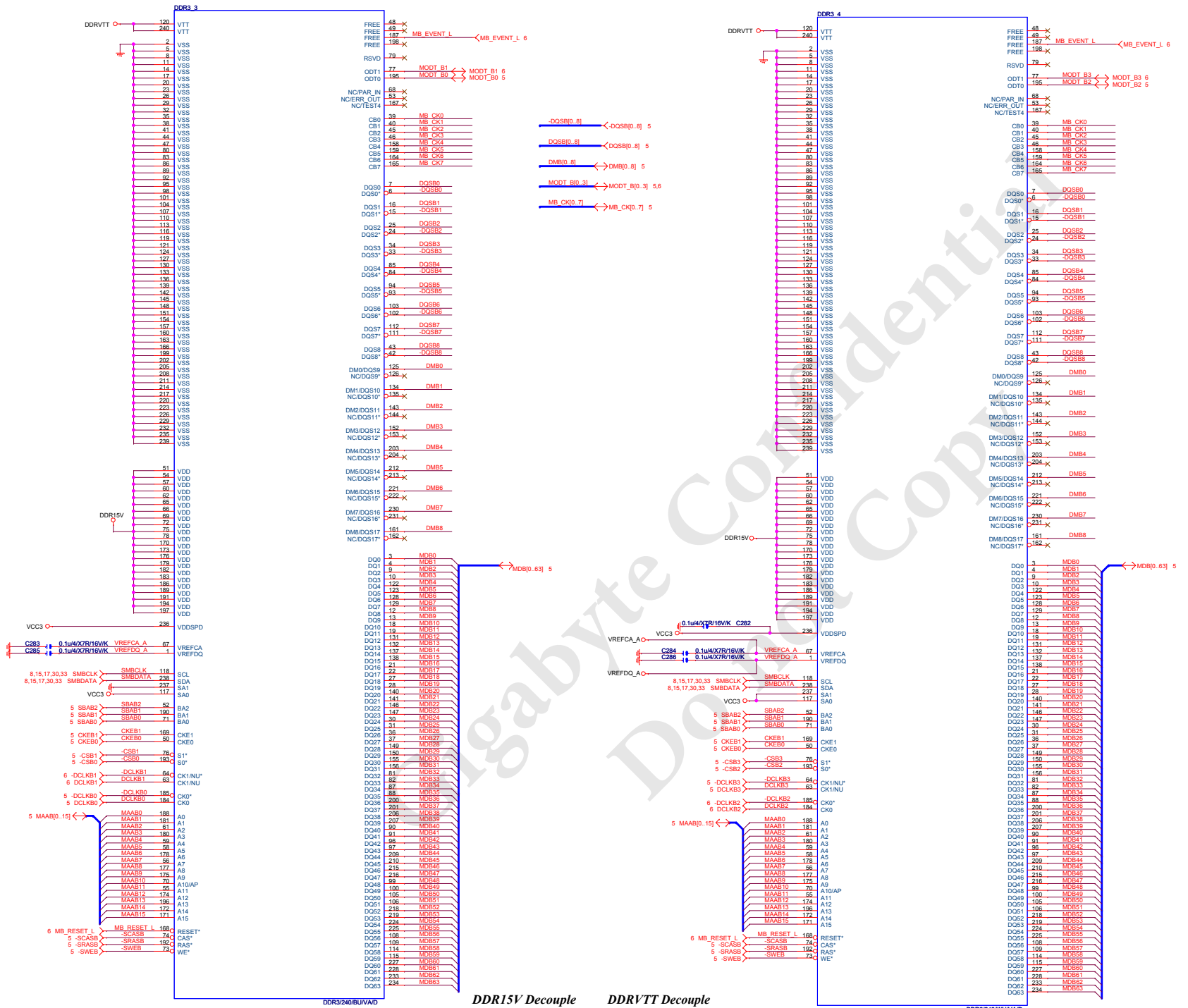








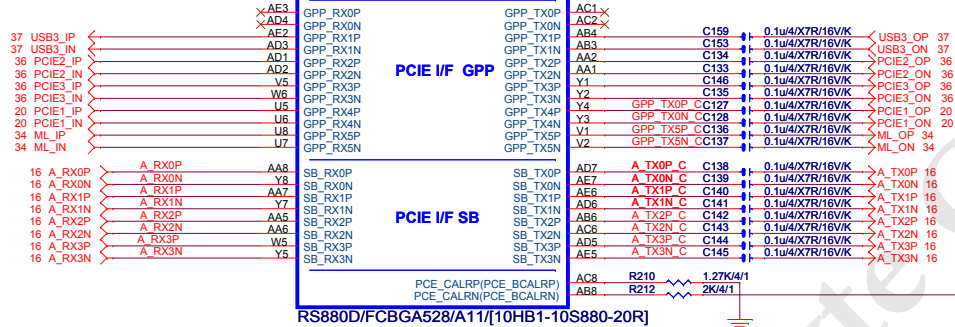
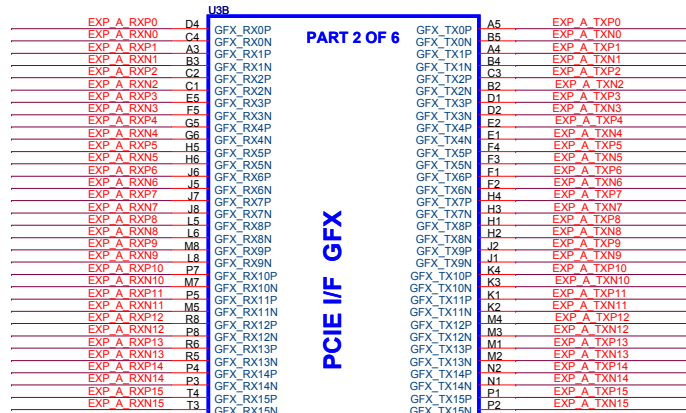




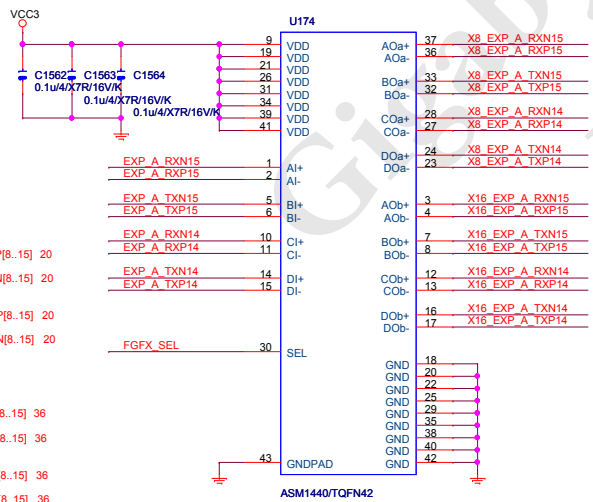
DDR15V Decouple      DDRVTT Decouple



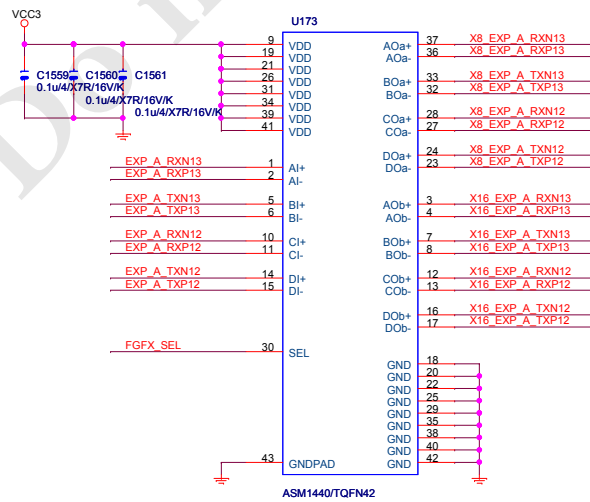
EXP\_A\_RXP[0..7] >>> EXP\_A\_RXP[0..7] 20  
EXP\_A\_RXN[0..7] >>> EXP\_A\_RXN[0..7] 20  
EXP\_A\_TXP[0..7] >>> EXP\_A\_TXP[0..7] 20  
EXP\_A\_TXN[0..7] >>> EXP\_A\_TXN[0..7] 20



RS880D/FCBGA528/A11/[10HB1-10S880-20R]



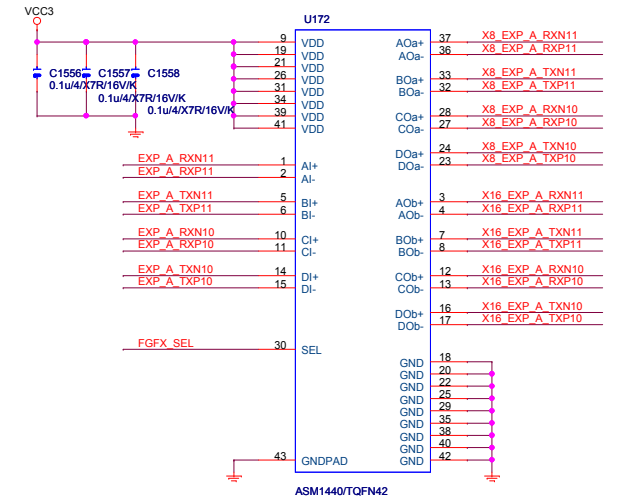
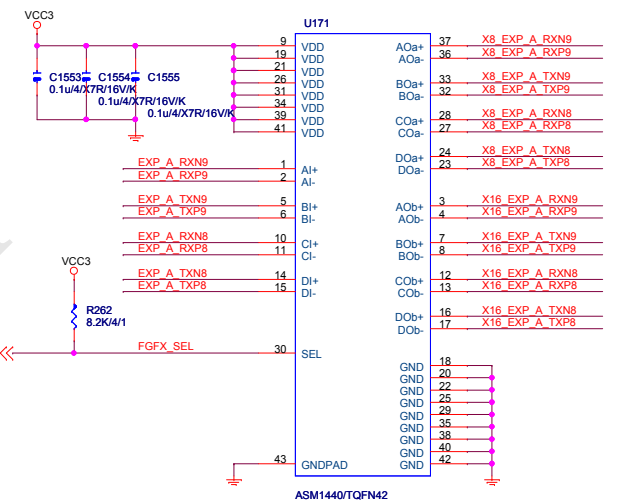
X16\_EXP\_A\_TXP[8..15] >>> X16\_EXP\_A\_TXP[8..15] 20  
X16\_EXP\_A\_TXN[8..15] >>> X16\_EXP\_A\_TXN[8..15] 20  
X16\_EXP\_A\_RXP[8..15] >>> X16\_EXP\_A\_RXP[8..15] 20  
X16\_EXP\_A\_RXN[8..15] >>> X16\_EXP\_A\_RXN[8..15] 20  
X8\_EXP\_A\_TXP[8..15] >>> X8\_EXP\_A\_TXP[8..15] 36  
X8\_EXP\_A\_TXN[8..15] >>> X8\_EXP\_A\_TXN[8..15] 36  
X8\_EXP\_A\_RXP[8..15] >>> X8\_EXP\_A\_RXP[8..15] 36  
X8\_EXP\_A\_RXN[8..15] >>> X8\_EXP\_A\_RXN[8..15] 36



PLACE CAP CLOSE TO CONNECTOR

NB\_VCC

Function	SEL
xI--> xOa	L ( X8 )
xI--> xOb	H ( X16 )



**GIGABYTE**™

Title  
**RS880 PCIE I/F Switch**

Size Custom Document Number  
**GA-890GPA-UD3H**

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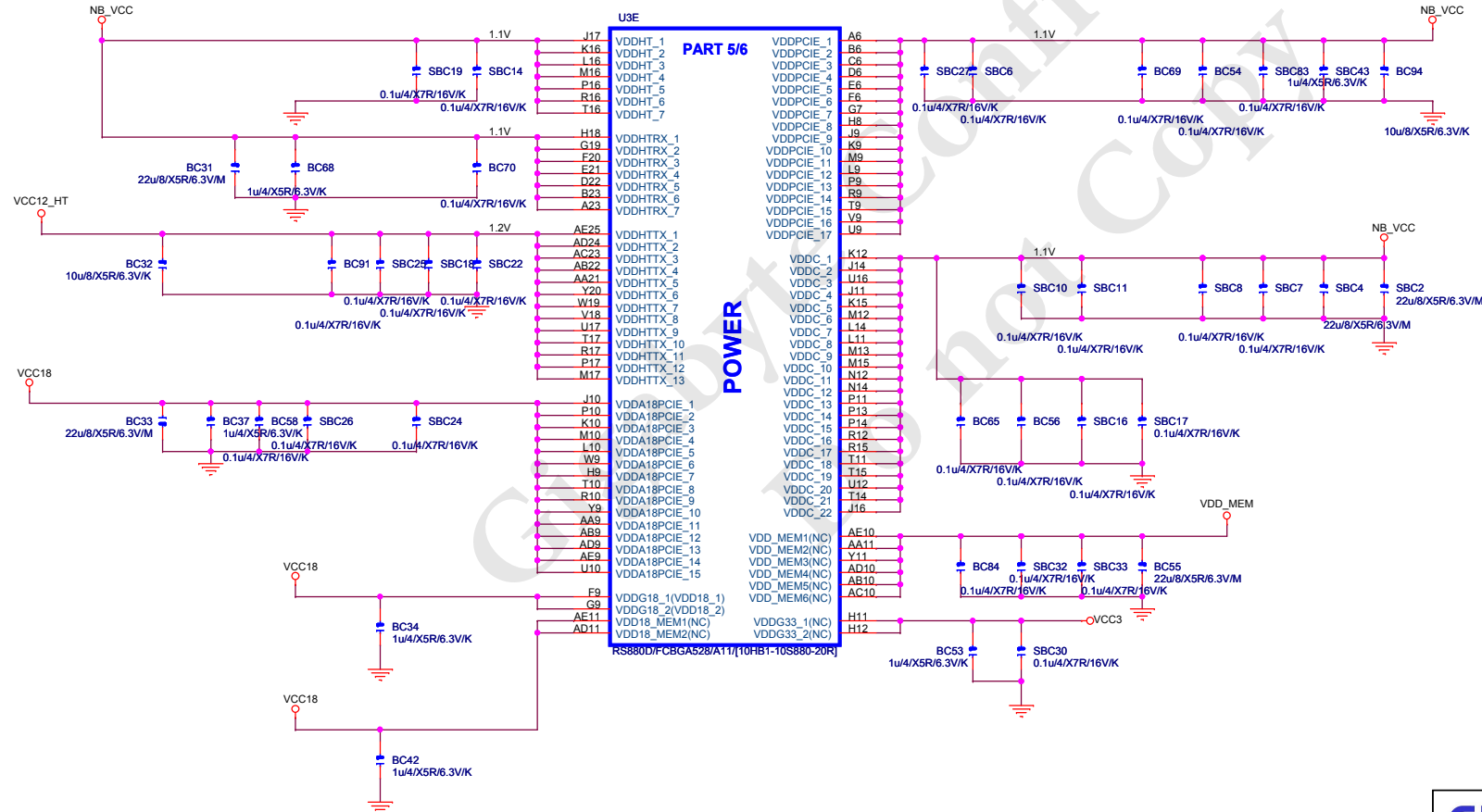
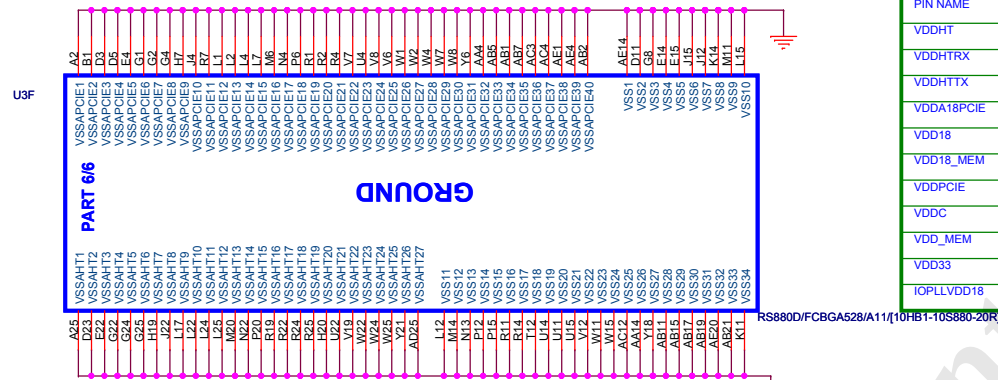
Rev  
**2.11**





### RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD0	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD0	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD018	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVD018	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC







- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800  
R851 less than 100 mils away from R800/801  
route CPU clock as 100ohm differential pair

## NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

\* the GFX\_REFCLK input is required for all cases

Parallel Resonance Crystal

watch dog --  
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Pin1: High=>DOC input, Low=>SRC5

**GIGABYTE**™

File  
**ICS9LPRS477**

Size  
Custom  
Document Number  
**GA-890GPA-UD3H**

Rev  
**2.11**

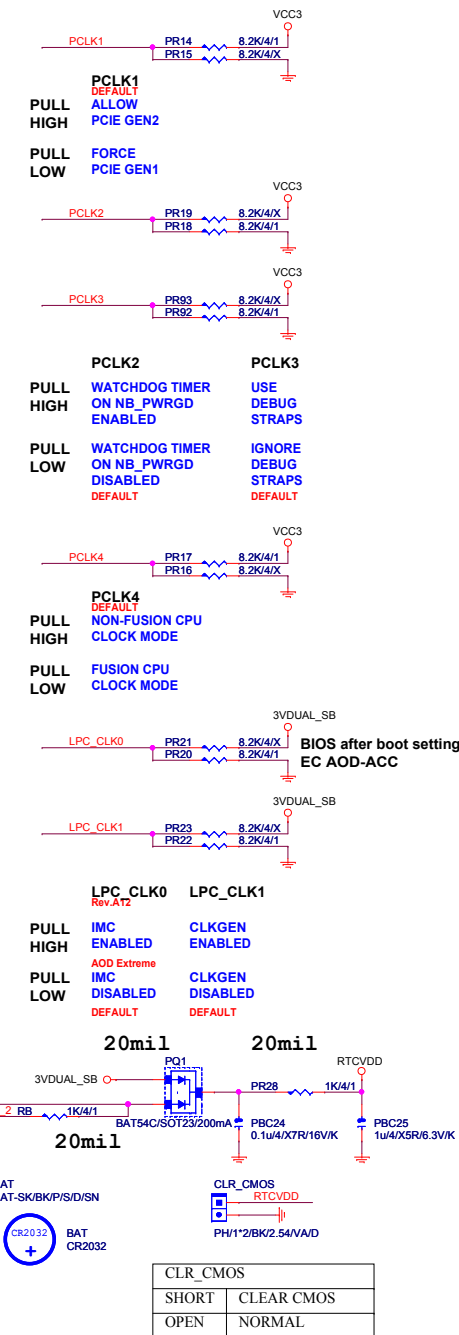
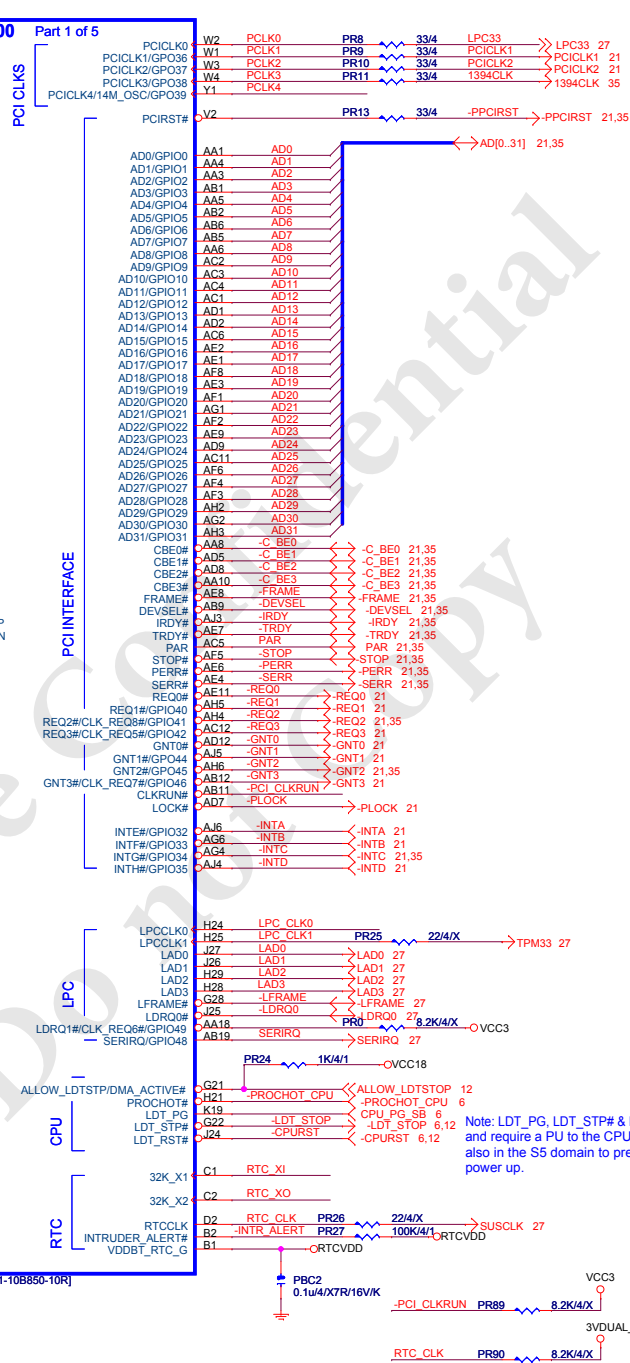
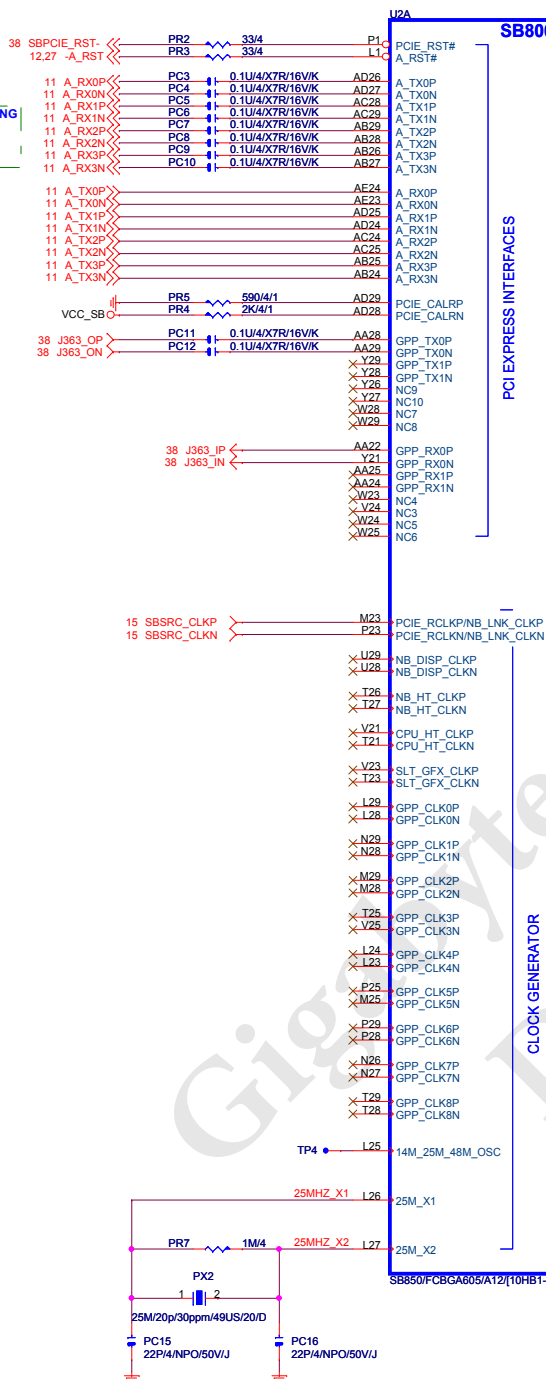
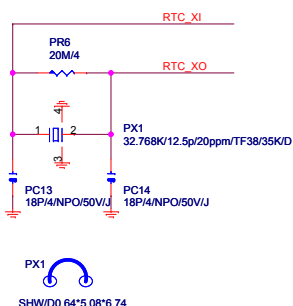
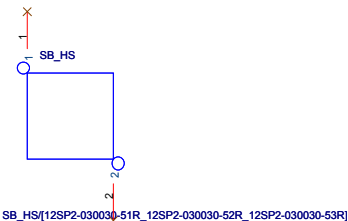
Date: Tuesday, June 15, 2010

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S.B HEATSINK



NOT ADD ICT FOR RTCVDD PIN

**GIGABYTE**

Title			
<b>ATI SB850 PCIE/PCI/CPU/LPC</b>			
Size	Document Number	Rev	
Custom	<b>GA-890GPA-UD3H</b>	<b>2.11</b>	
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SB TEST2 PR29 8.2K/4/1  
SB TEST1 PR30 8.2K/4/1  
SB TEST0 PR31 8.2K/4/1

-SUS\_STAT PR32 8.2K/4/1  
SMBCLK PR55 1K/4/1  
SMBDATA PR56 1K/4/1  
WD\_PWRGD PR33 8.2K/4/1

-RI PR34 8.2K/4/1  
SMBCLK1 PR57 2.2K/4/1  
SMBDATA1 PR58 2.2K/4/1  
-PCIE\_WAKE PR59 2.2K/4/1  
-PCIPME PR60 2.2K/4/1

SB\_PWR0K PR64 100P/4/NPO/50V/JX  
3VDUAL\_SB PR91 20K/4/1

SMBCLK PR65 100P/4/NPO/50V/JX  
SMBDATA PR66 100P/4/NPO/50V/JX

AZ\_BIT\_CLK PR67 100P/4/NPO/50V/JX

AZ\_SDATA\_OUT PR36 8.2K/4/1  
PR35 8.2K/4/1

-AZ\_RST PR37 8.2K/4/1X

Low: Disable PCI MEM boot(D),  
Up: Enable PCI MEM boot

AZ\_SDOUT  
PULL HIGH  
LOW POWER  
MODE  
PULL LOW  
PERFORMANCE  
MODE  
DEFAULT

21.35 -PCIPME 24 -RI  
27.31.33 -SLP\_S3  
31 SLP\_S5  
27 -PSOUT PR69 0/4/SHT/X-PWRBTN  
31 SB\_PWR0K  
12 -SUS\_STAT

SB TEST2  
SB TEST1  
SB TEST0

27 A20GATE  
27.29 -KBRS1  
27 -LPCPME  
27 GP53

36 PE4\_PRSENT-  
20 PE0\_PRSENT- PR83 0/4/X

29 SPKR  
8.9,15,30,33 SMBCLK  
8.9,15,30,33 SMBDATA  
20,36 SMBCLK1  
20,36 SMBDATA1

VDD\_MEM PR38 8.2K/4/1  
DDR3\_RST-  
13 DDR3\_RST-

37 SMIB  
35.37 -USBOC\_R1  
24 -USBOC\_F1

25 AZ\_BIT\_CLK PR63 22/4  
25 AZ\_SDATA\_OUT PR64 22/4  
25 AZ\_SDATA\_IN0  
25 AZ\_SYNC PR65 22/4  
25 -AZ\_RST PR66 22/4

PR39 8.2K/4/1 GBE\_COL  
PR40 8.2K/4/1 GBE\_CRS  
3VDUAL PR41 8.2K/4/1 GBE\_MDIO  
PR42 8.2K/4/1 GBE\_RXERR  
3VDUAL PR43 8.2K/4/1 GBE\_INTR

PS2\_DAT/SDA4/GPIO187  
PS2\_CLK/SC4/GPIO188  
SPI\_CS2#/GBE\_STAT2/GPIO166  
FC\_RST#/GPO160  
PS2KB\_DAT/GPIO189  
PS2KB\_CLK/GPIO190  
PS2M\_DAT/GPIO191  
PS2M\_CLK/GPIO192

GBE\_COL  
GBE\_CRS  
GBE\_MDCK  
GBE\_MDIO  
GBE\_RXCLK  
GBE\_RXD3  
GBE\_RXD2  
GBE\_RXD1  
GBE\_RXD0  
GBE\_RXCTL/RXDV  
GBE\_RXERR  
GBE\_TXCLK  
GBE\_TXD3  
GBE\_TXD2  
GBE\_TXD1  
GBE\_TXD0  
GBE\_TXCTL/TXEN  
GBE\_PHY\_PD  
GBE\_PHY\_RST#  
GBE\_PHY\_INTR

PS2\_DAT/SDA4/GPIO187  
PS2\_CLK/SC4/GPIO188  
SPI\_CS2#/GBE\_STAT2/GPIO166  
FC\_RST#/GPO160  
PS2KB\_DAT/GPIO189  
PS2KB\_CLK/GPIO190  
PS2M\_DAT/GPIO191  
PS2M\_CLK/GPIO192

PS2\_DAT/SDA4/GPIO187  
PS2\_CLK/SC4/GPIO188  
SPI\_CS2#/GBE\_STAT2/GPIO166  
FC\_RST#/GPO160  
PS2KB\_DAT/GPIO189  
PS2KB\_CLK/GPIO190  
PS2M\_DAT/GPIO191  
PS2M\_CLK/GPIO192

PS2\_DAT/SDA4/GPIO187  
PS2\_CLK/SC4/GPIO188  
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PS2M\_CLK/GPIO192

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PS2M\_DAT/GPIO191  
PS2M\_CLK/GPIO192

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FC\_RST#/GPO160  
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PS2KB\_CLK/GPIO190  
PS2M\_DAT/GPIO191  
PS2M\_CLK/GPIO192

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PS2\_CLK/SC4/GPIO188  
SPI\_CS2#/GBE\_STAT2/GPIO166  
FC\_RST#/GPO160  
PS2KB\_DAT/GPIO189  
PS2KB\_CLK/GPIO190  
PS2M\_DAT/GPIO191  
PS2M\_CLK/GPIO192

PS2\_DAT/SDA4/GPIO187  
PS2\_CLK/SC4/GPIO188  
SPI\_CS2#/GBE\_STAT2/GPIO166  
FC\_RST#/GPO160  
PS2KB\_DAT/GPIO189  
PS2KB\_CLK/GPIO190  
PS2M\_DAT/GPIO191  
PS2M\_CLK/GPIO192

USBCLK/14M\_25M\_48M\_OSC  
USB\_RCOMP  
USB\_FSD1P/GPIO186  
TEST0  
USB\_FSD0P/GPIO185  
USB\_FSDON

USB\_HSD13P  
USB\_HSD13N  
USB\_HSD12P  
USB\_HSD12N  
USB\_HSD11P  
USB\_HSD11N

USB\_HSD10P  
USB\_HSD10N  
USB\_HSD9P  
USB\_HSD9N  
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USB\_HSD8N

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USB\_HSD1N

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USB\_HSD0P  
USB\_HSD0N

**GIGABYTE**™

Title: **ATI SB850 ACPI/USB/GPIO/AUDIO**

Size: Custom Document Number: **GA-890GPA-UD3H** Rev: **2.11**

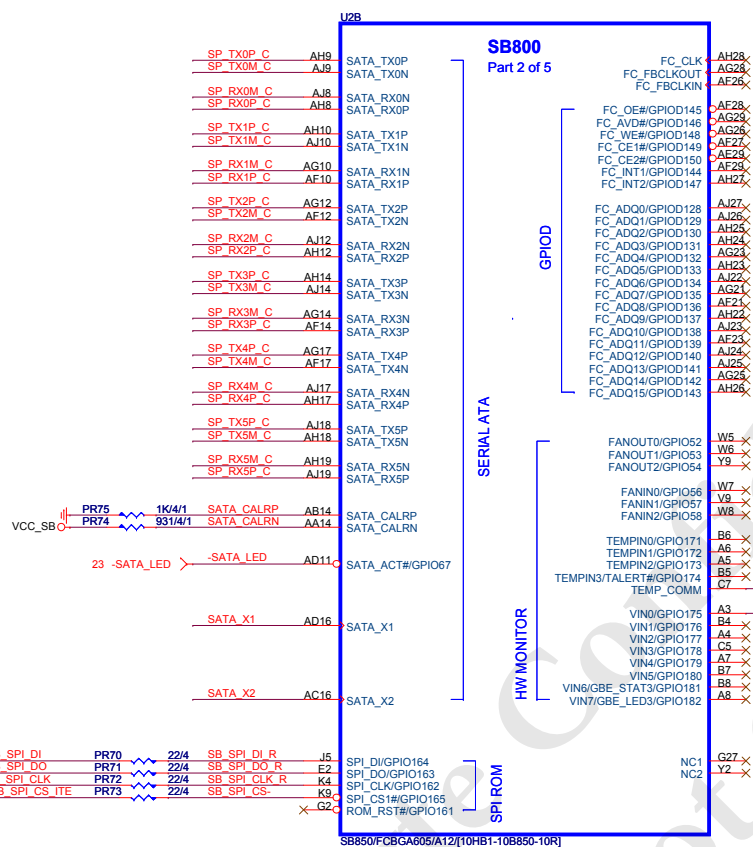
Date: Tuesday, June 15, 2010 Sheet 17 of 38



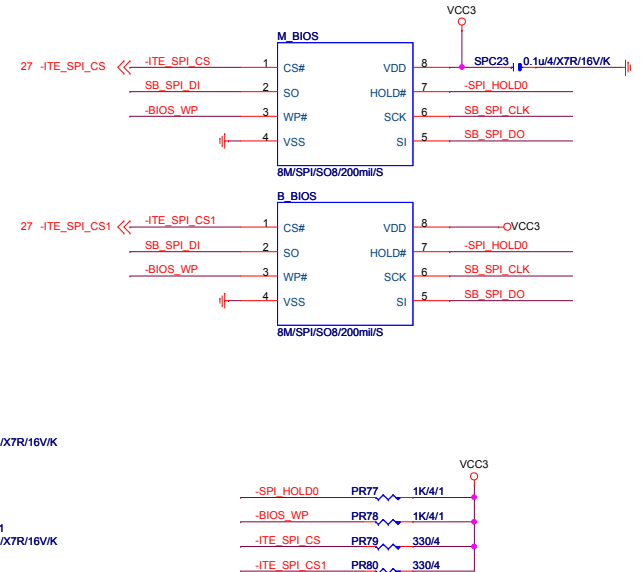
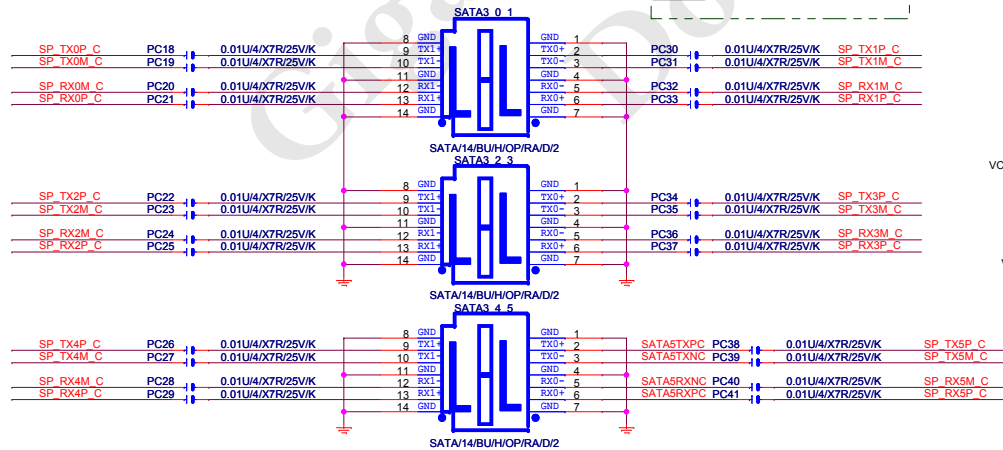
PLACE SATA\_CAL  
RES VERY CLOSE  
TO BALL OF U600

**NOTE :**

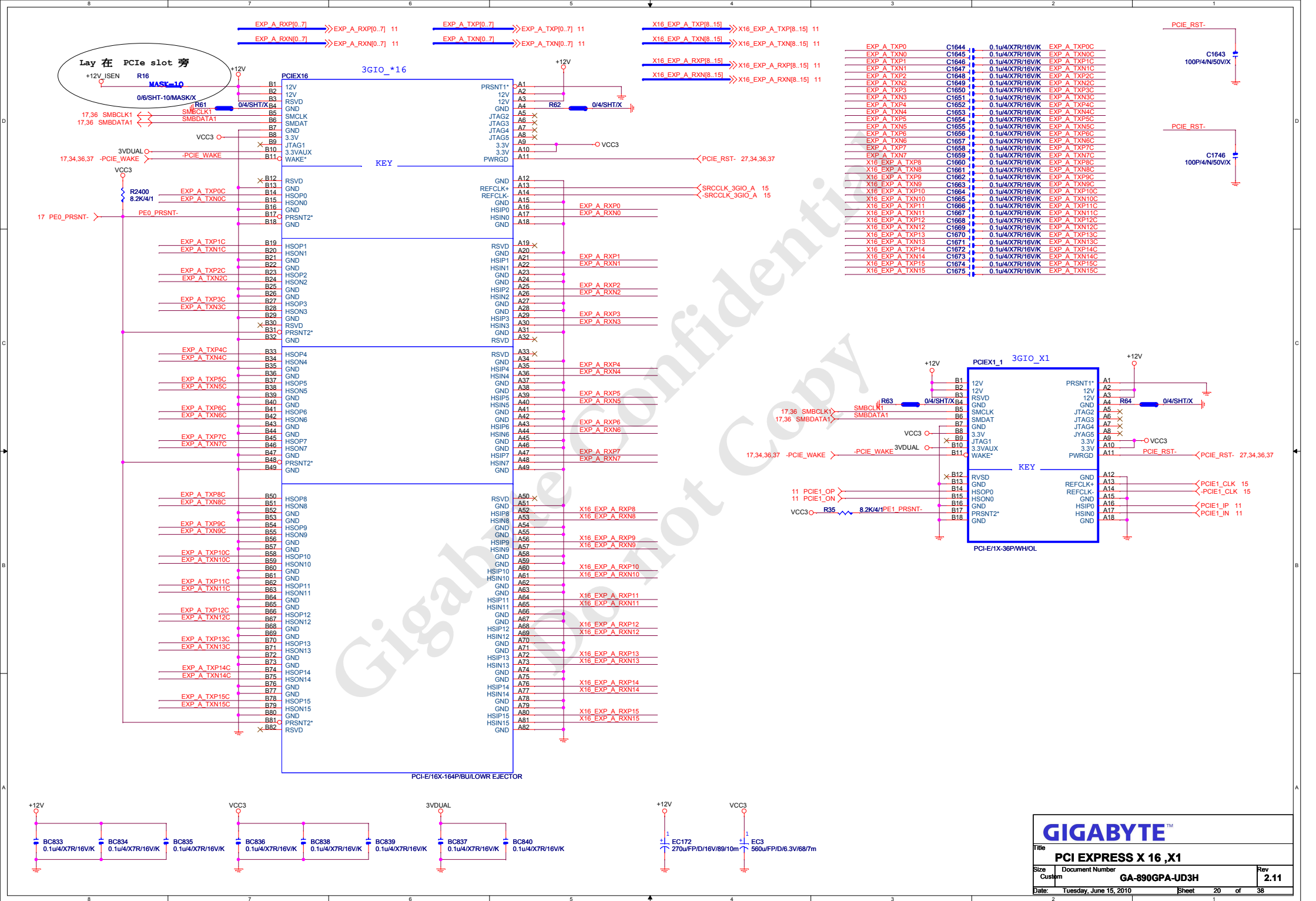
R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



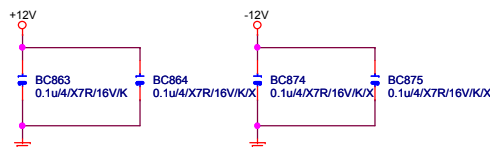
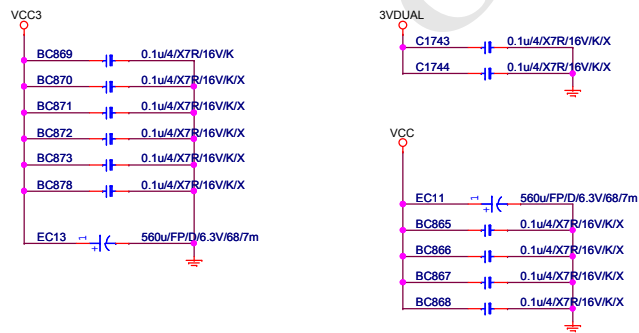
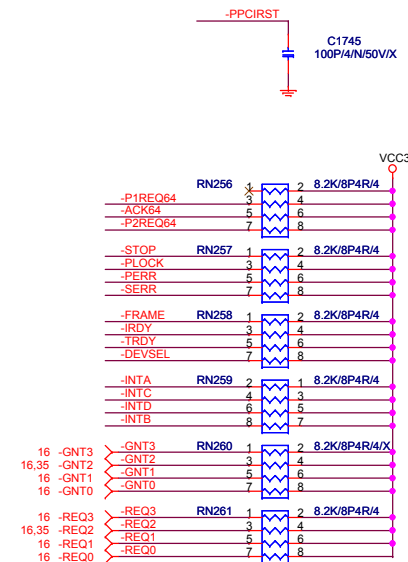
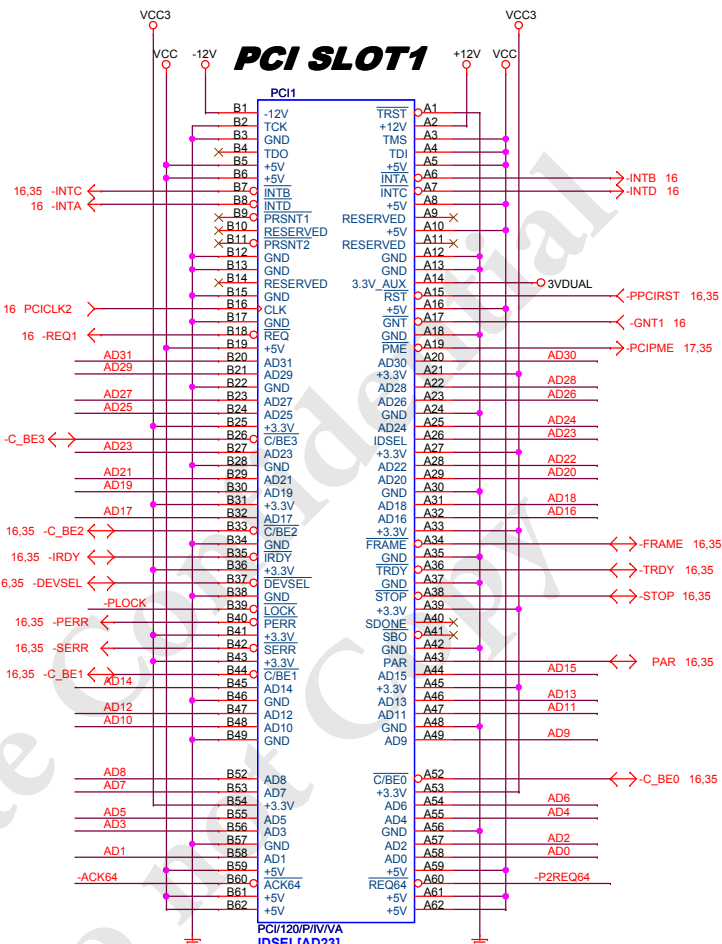
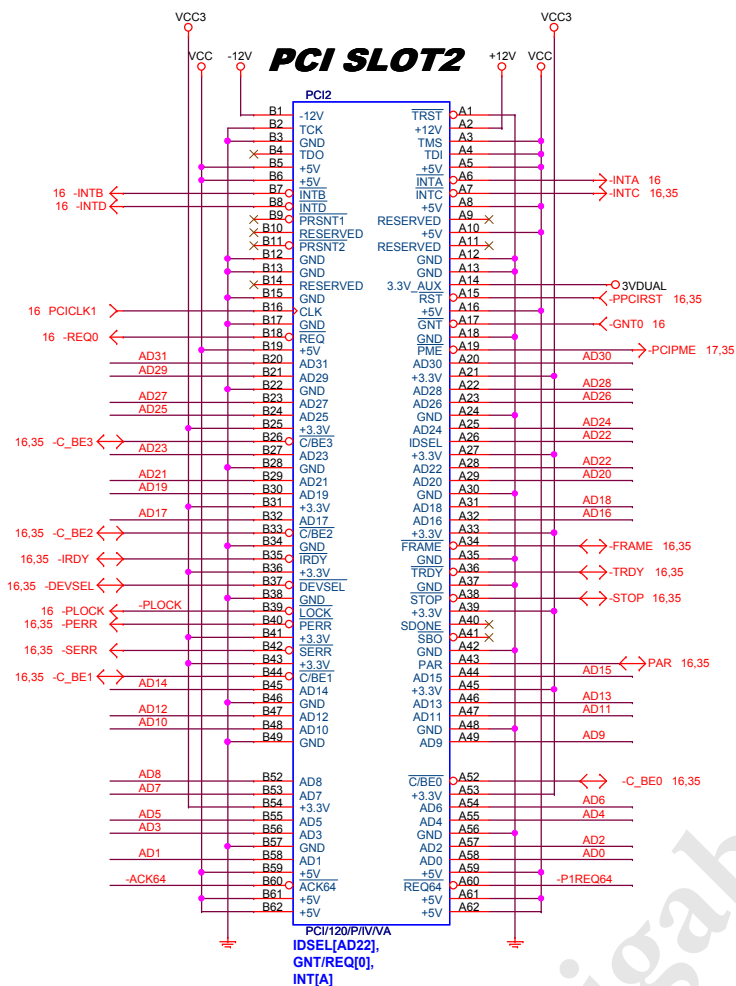
PLACE SATA AC COUPLING  
CAPS CLOSE TO SB850

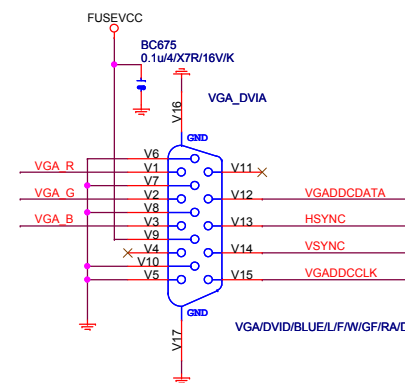
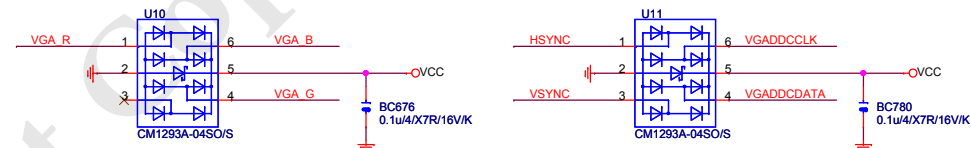
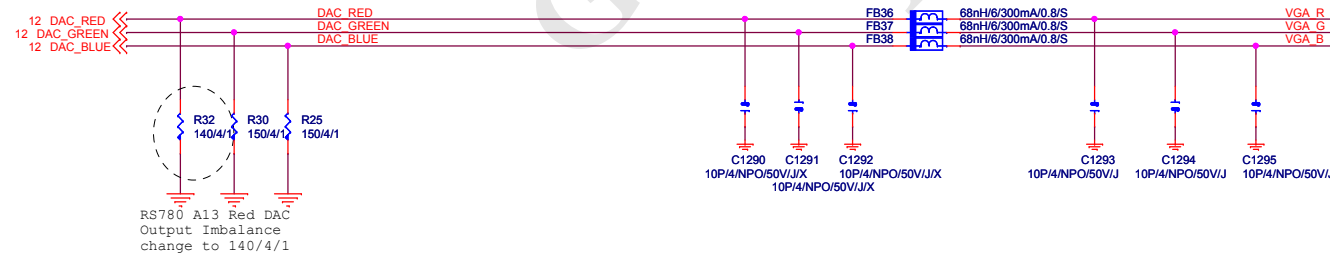
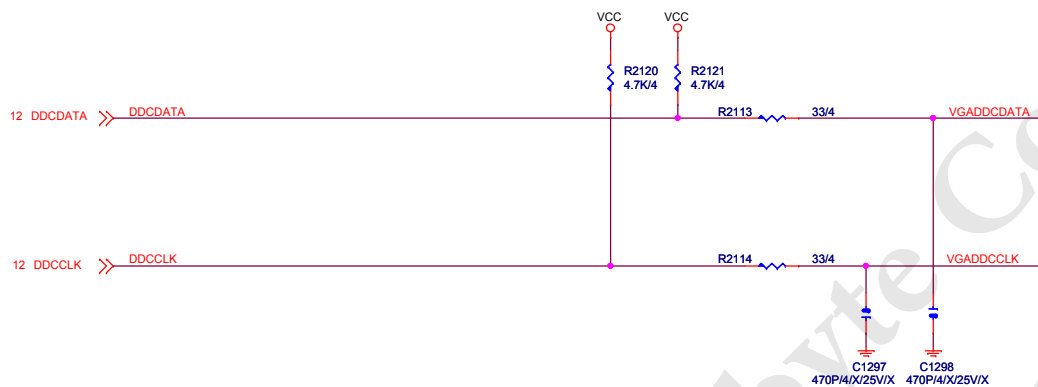
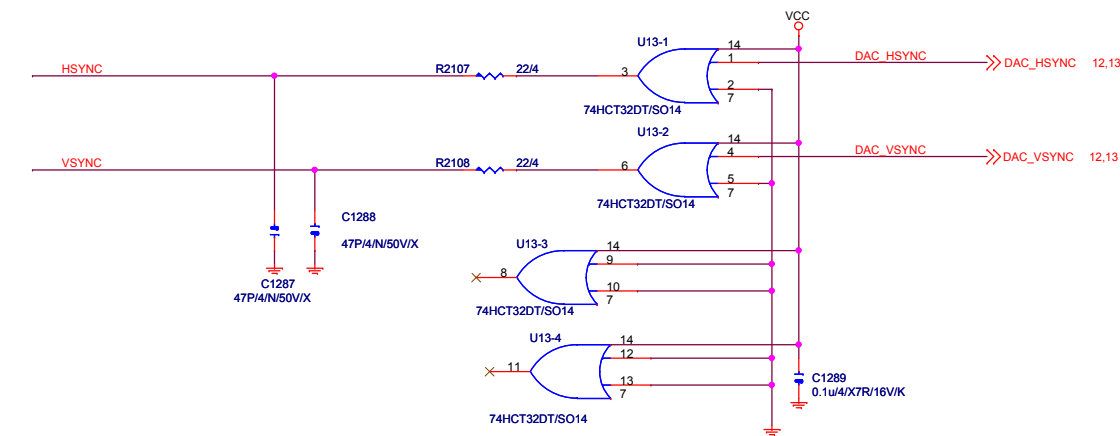




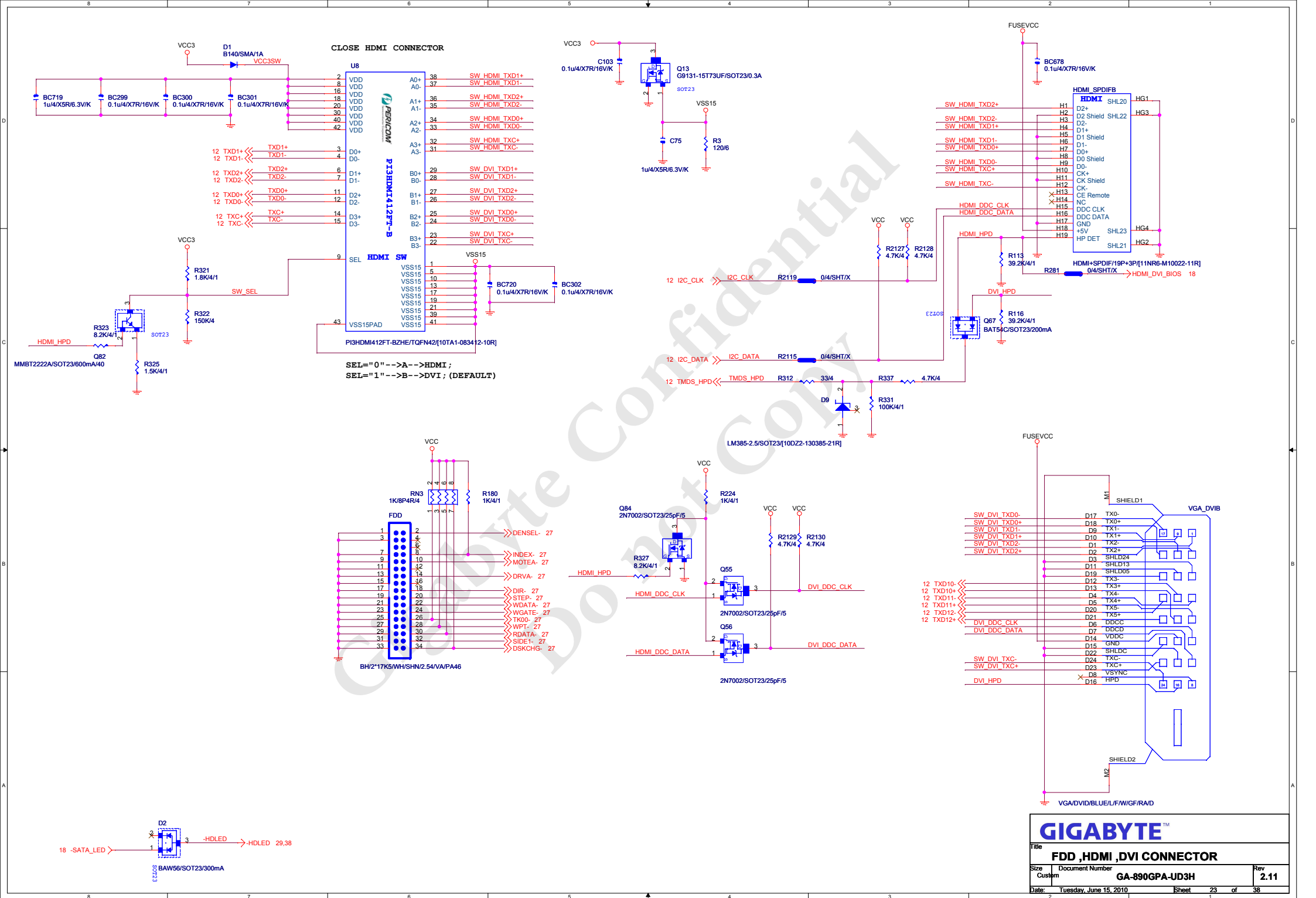






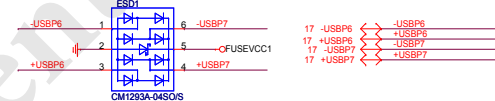
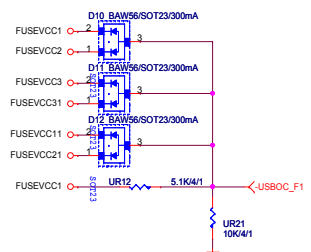
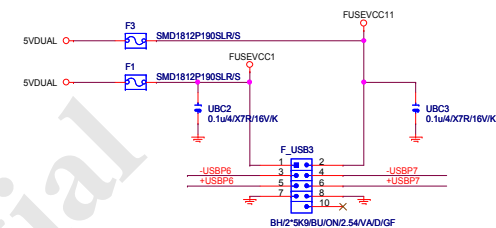




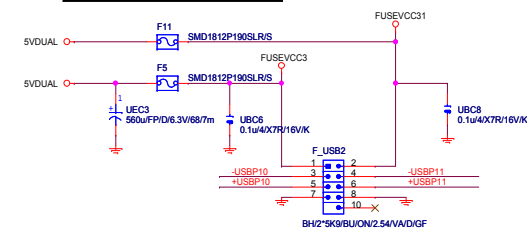




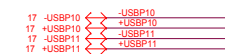
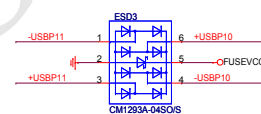
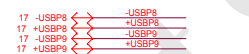
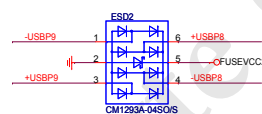
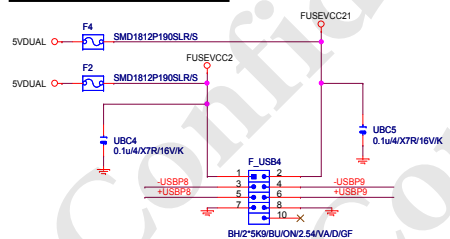
## FRONT SIDE USB3



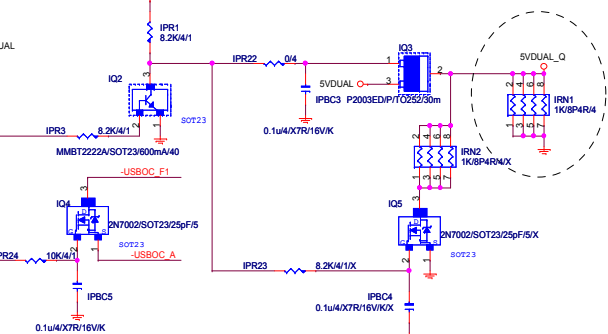
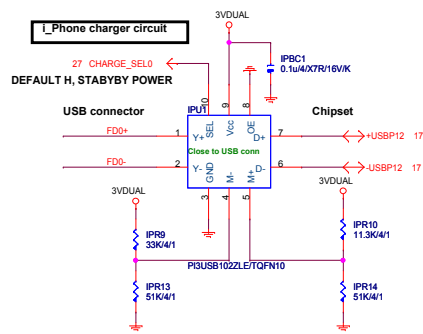
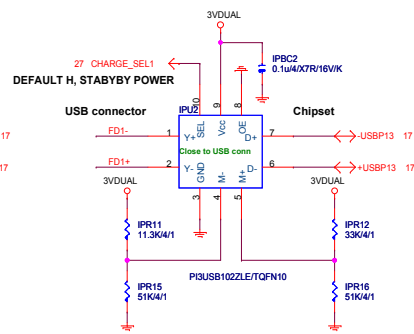
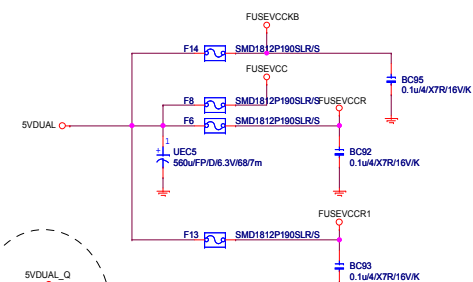
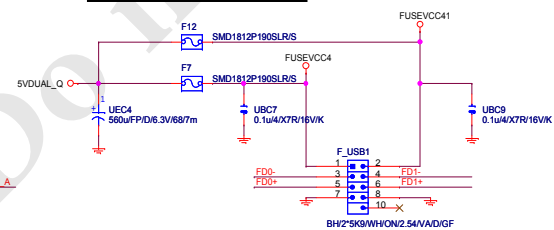
## FRONT SIDE USB2



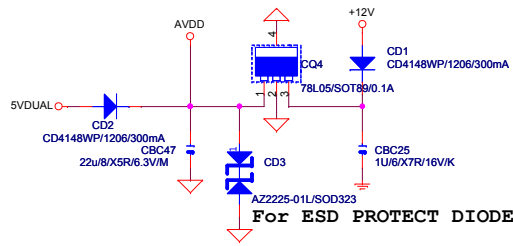
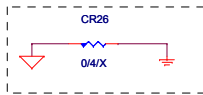
## FRONT SIDE USB4



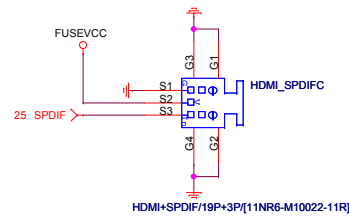
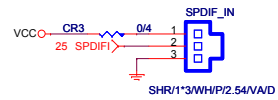
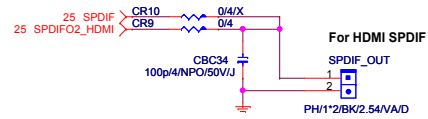
## FRONT SIDE USB1



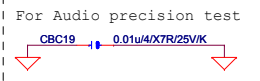
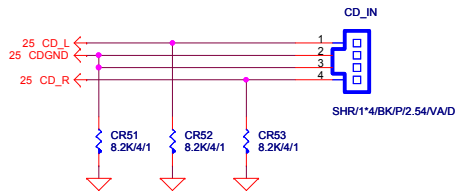




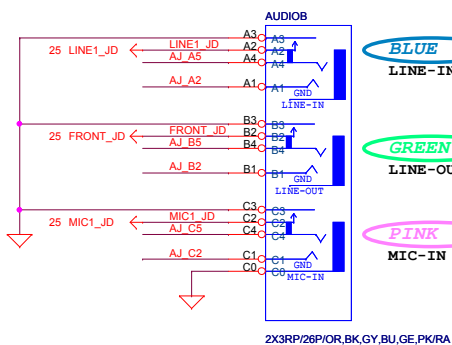
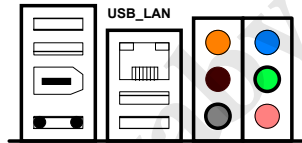
## SPDIF



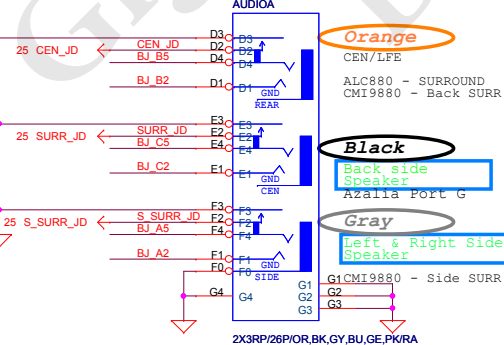
## CD IN



## USB\_1394\_ESATA

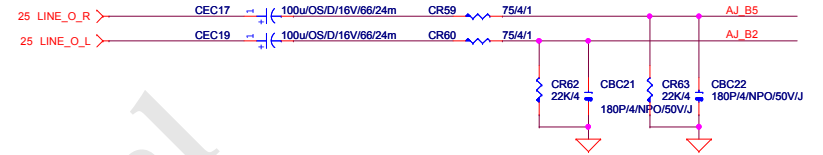


A3R3/13P/B/[11NR6-403006-01\_11NR6-403006-02]  
3R3+15P/[11NR6-403004-11]

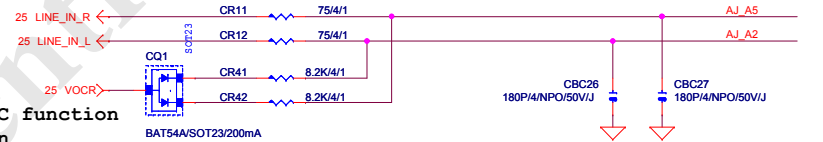


A3R3/13P/B/[11NR6-403006-71]  
3R3+15P/[11NR6-403004-31]

## LINE OUT FRONT OUT

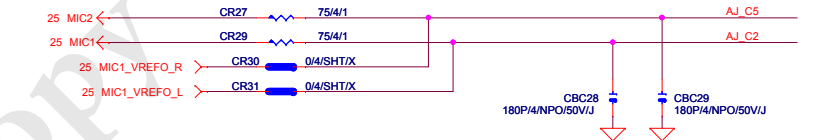


## LINE-IN

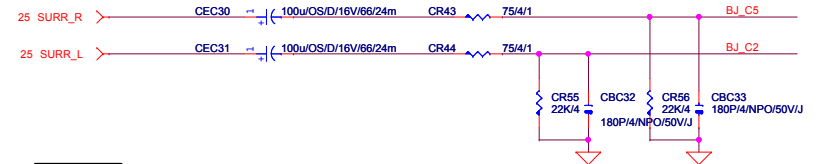


Verify MIC function  
in LINE-in

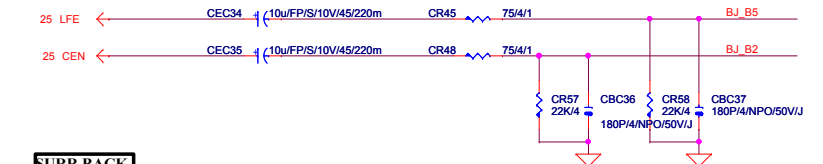
## MIC



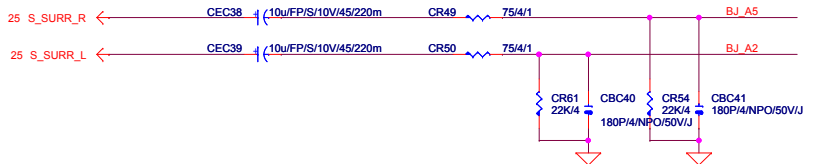
## SURROUND



## CEN/LFE

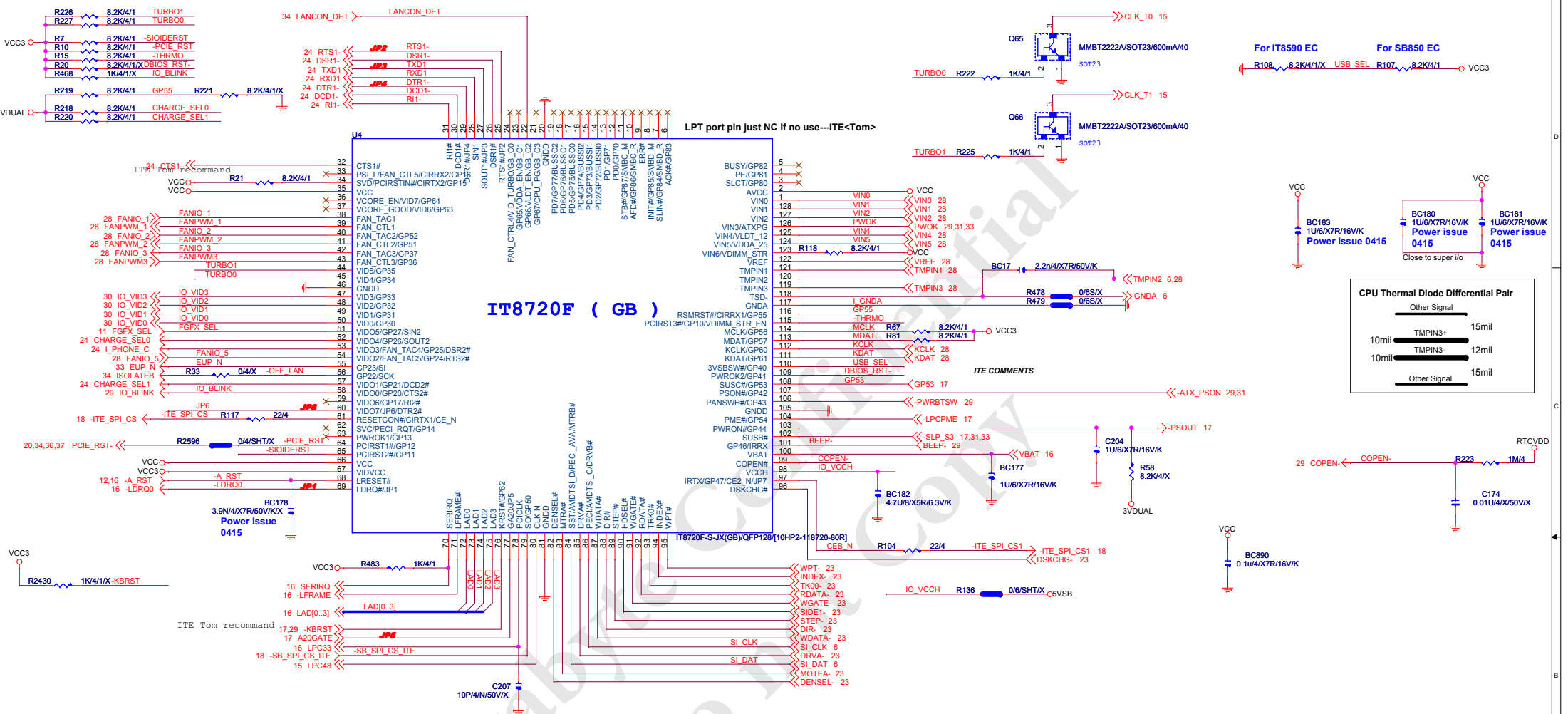


## SURR BACK

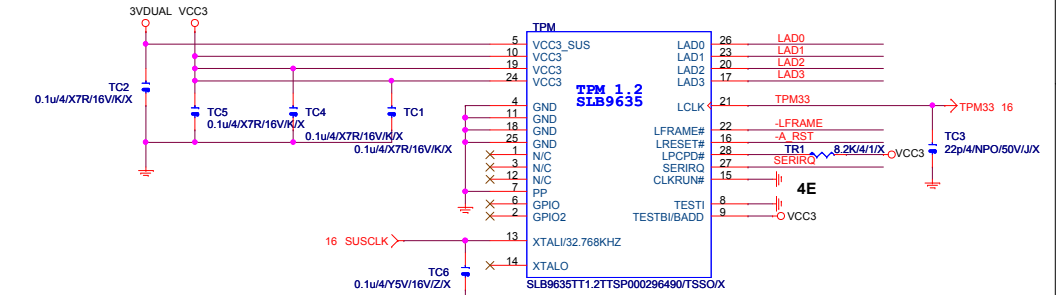
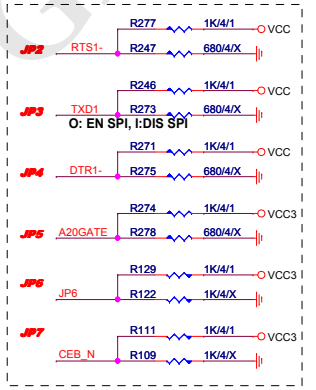


**GIGABYTE**

Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	GA-890GPA-UD3H	2.11
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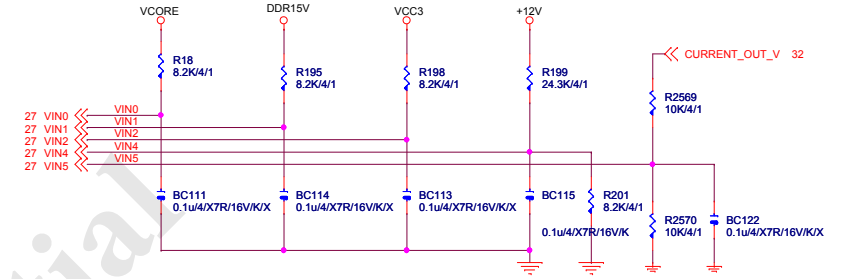
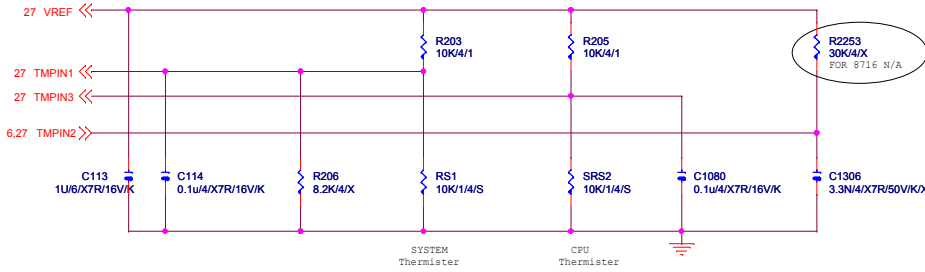
Symbol	value	Description
JP1		
Pin 69		
JP2	1	Disable VID output pins
Pin 25	0	Enable VID output pins
JP3	1	Disabled.
Pin 27	0	Flash I/F Address Segment 1 is enabled
JP4	1	K8 power sequence disabled
Pin 29	0	K8 power sequence enabled
JP3 & JP5	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
Pin 27 & Pin 77	10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
	01 Full Run	Default value of EC Index 15h/16h/17h is 00h
	00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5	1	Disable WDT to rest PWROK
Pin 77	0	Enable WDT to rest PWROK
JP6	1	Disable SVID Function
Pin 60	0	Enable SVID Function
JP7	1	Enable Dual BIOS Function for GigaByte Only
Pin 97	0	Disable Dual BIOS Function for GigaByte Only



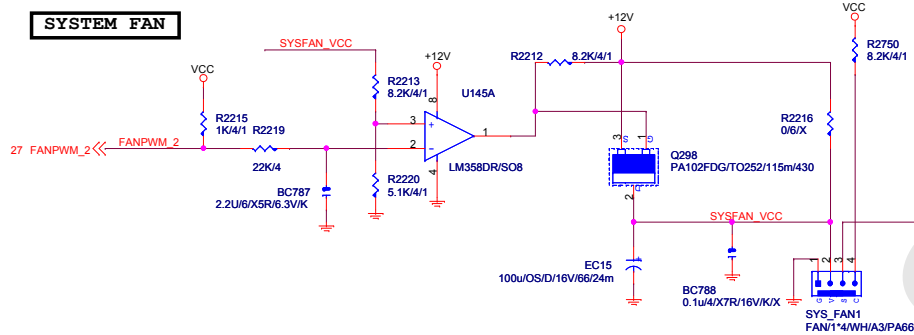
**GIGABYTE**<sup>TM</sup>

Title <b>ITE 8720 LPC IO, TPM</b>		
Size Custom	Document Number <b>GA-890GPA-UD3H</b>	Rev <b>2.11</b>
Date Tuesday, June 15, 2010	Sheet 27	of 38

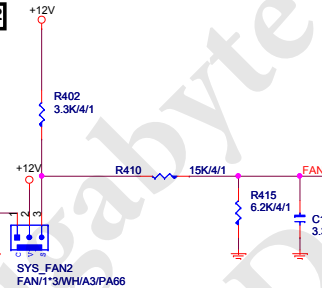
## Hardware Monitor circuits



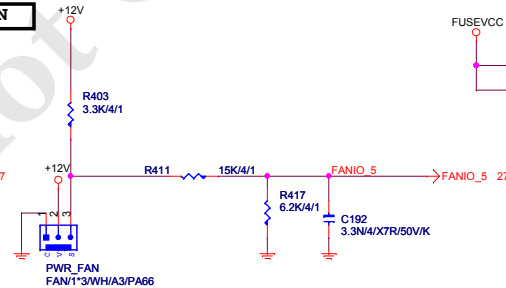
### SYSTEM FAN



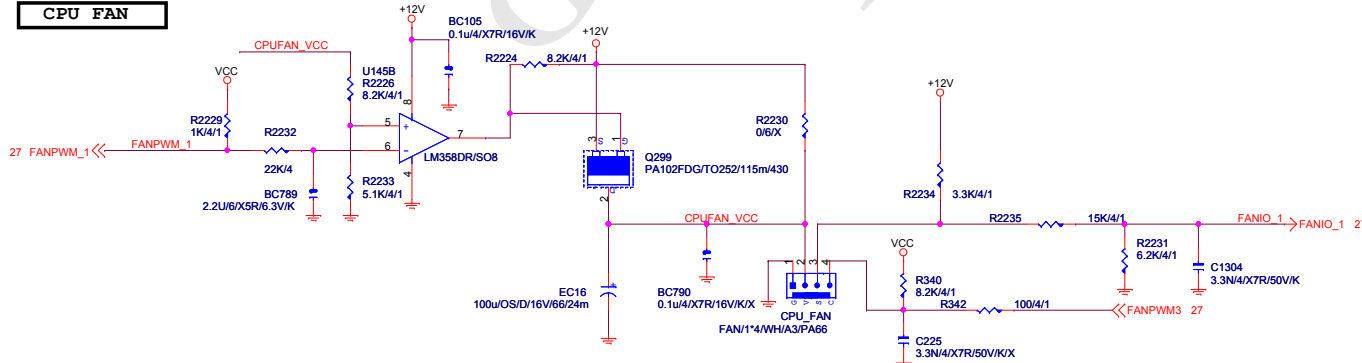
### SYSTEM FAN2



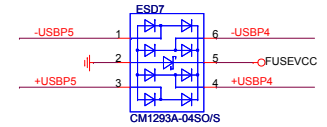
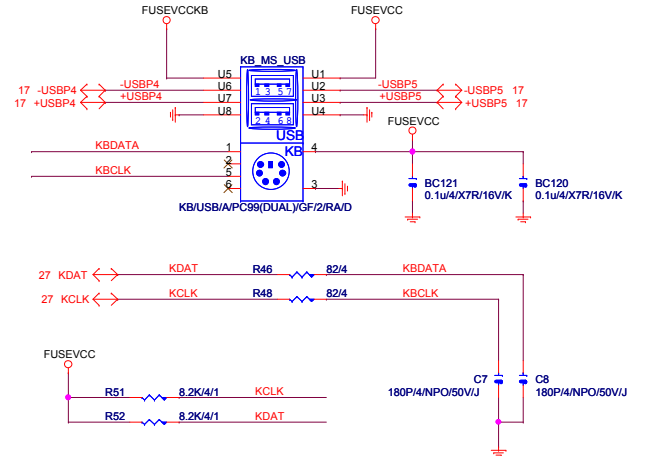
### POWER FAN



### CPU FAN

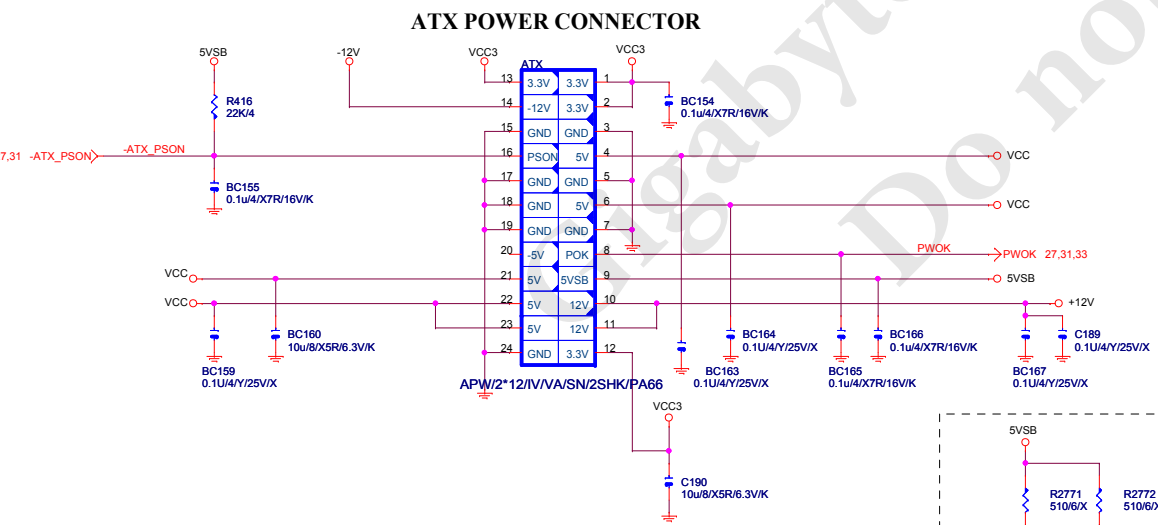
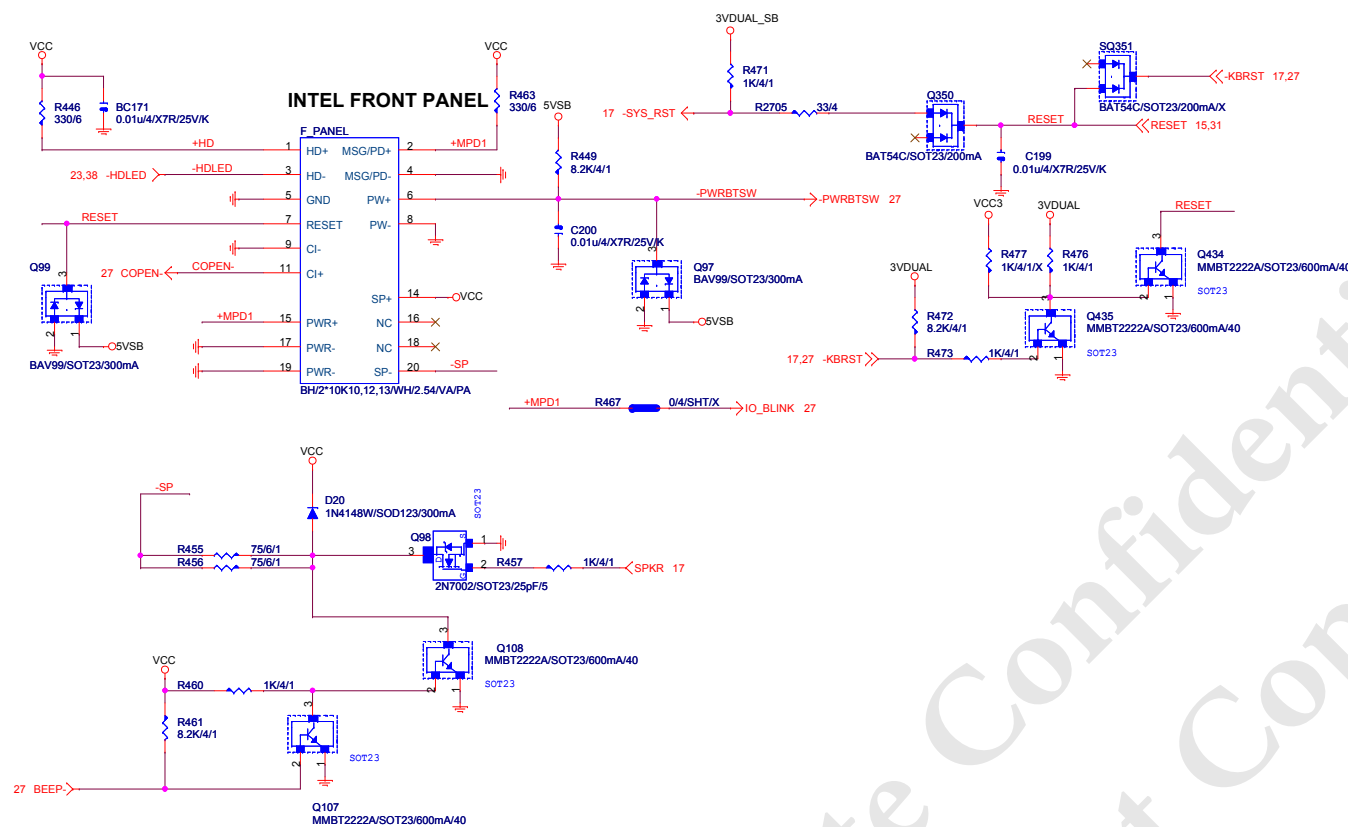


## KB & USB

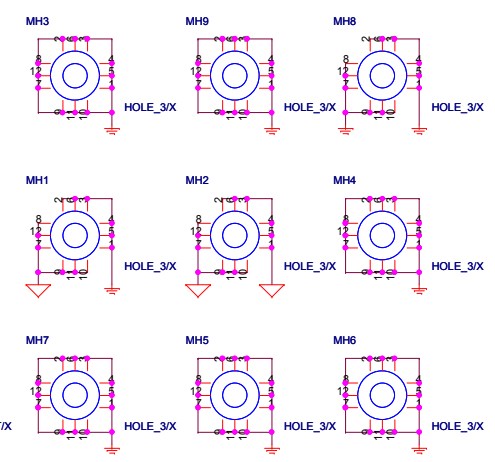
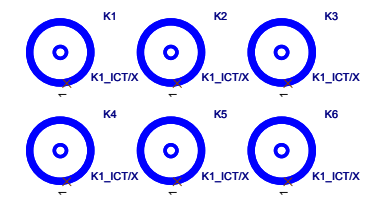
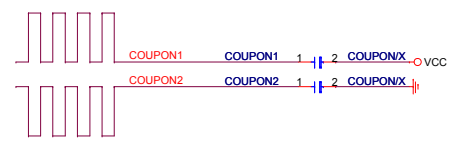


**GIGABYTE**

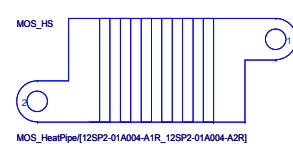
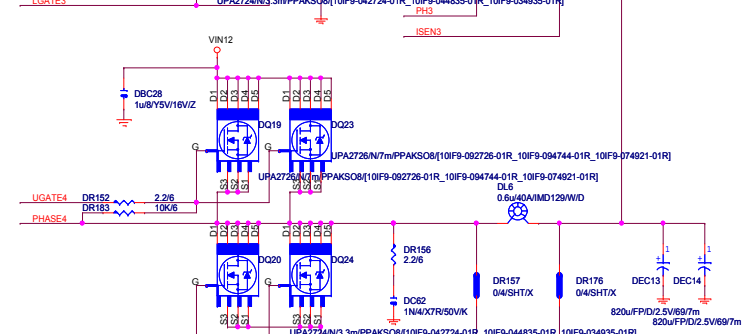
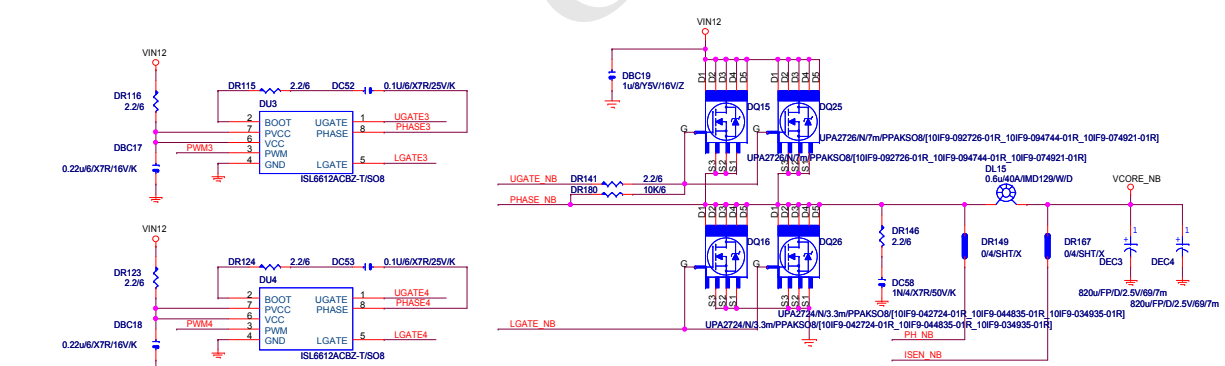
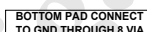
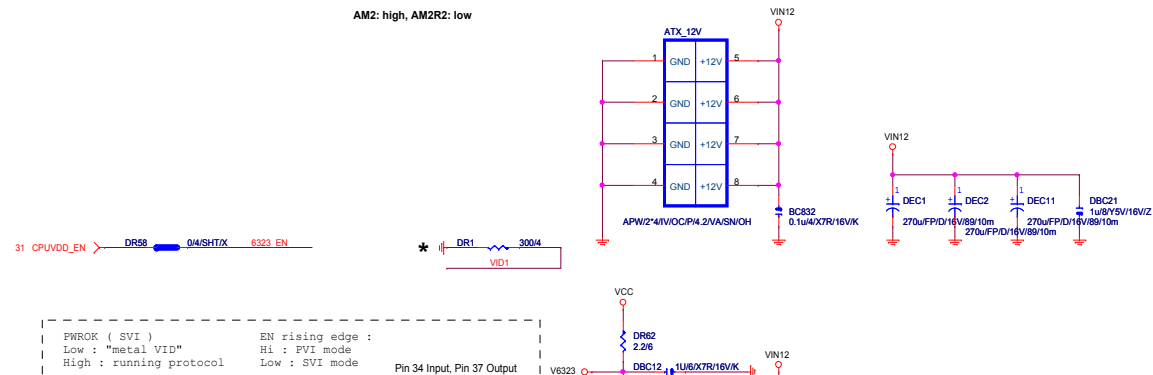
Title			FAN/HWMO KB/USB
Size	Document Number	Rev	2.11
Custom	GA-890GPA-UD3H		
Date:	Tuesday, June 15, 2010	Sheet	28 of 38



For Seasonic 900W  
 Power supply  
 cant Boot issue



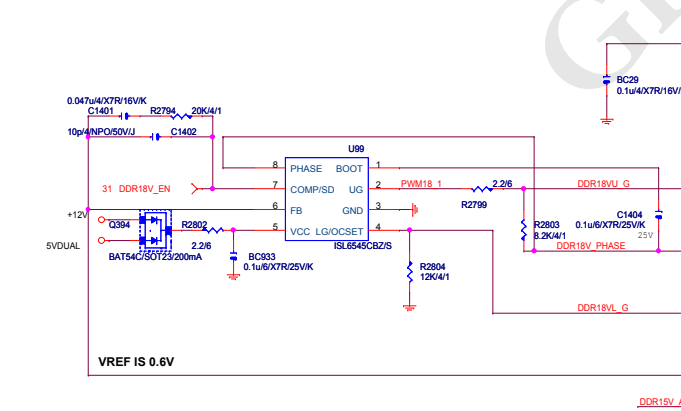
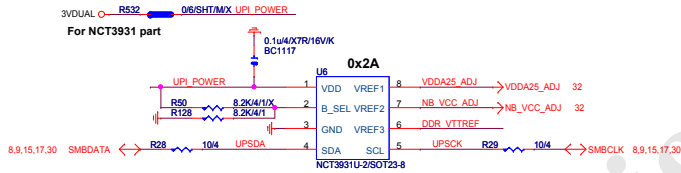
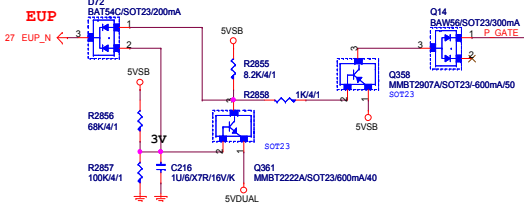
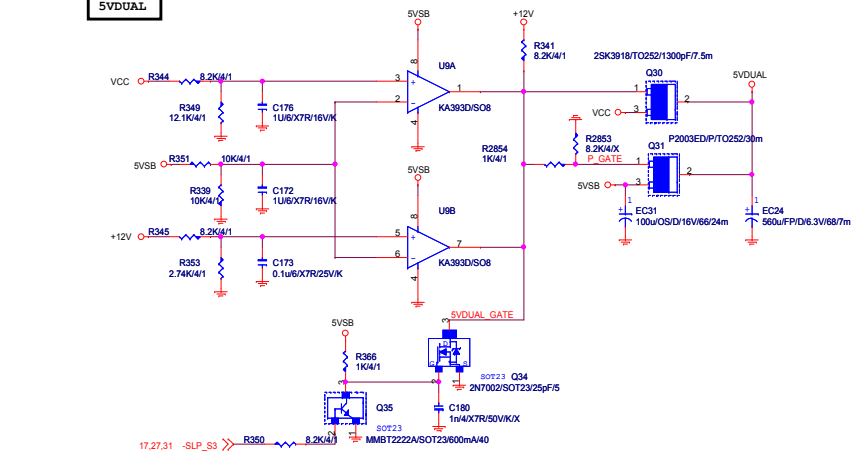




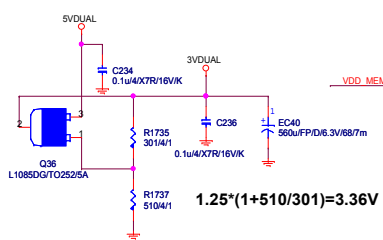




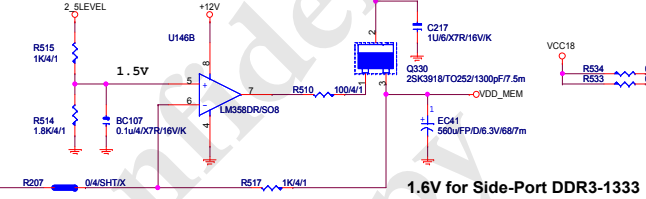
# 5VDUAL



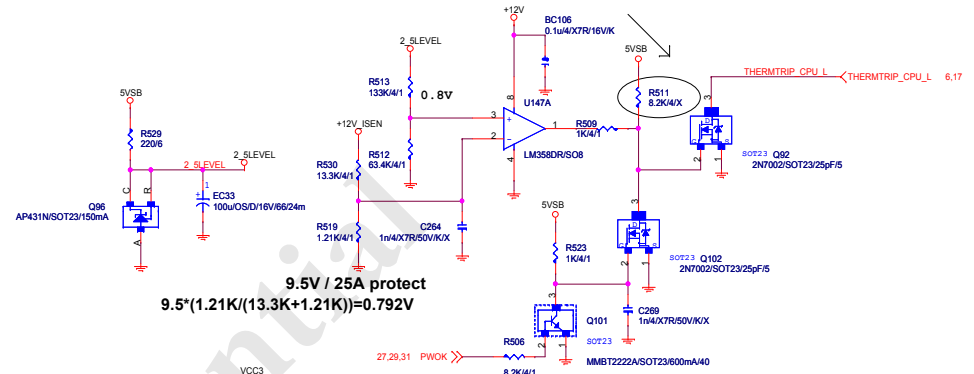
# 3VDUAL



# VDD\_MEM



R2038不能上,會導致U324 PIN1不能完全拉Lo



9.5V / 25A protect  
9.5\*(1.21K/(13.3K+1.21K))=0.792V

27.29.31 PWOK

VDD\_MEM

1.6V for Side-Port DDR3-1333

1.25\*(1+510/301)=3.36V

0.6\*(1+1.5K/1K)=1.5V

1.5V@20A

Default: 1.5V, from AMD

4 VIA to GND

4 VIA to GND

4 VIA to GND

4 VIA to GND

4 VIA to GND

4 VIA to GND

4 VIA to GND

4 VIA to GND

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4 VIA to GND

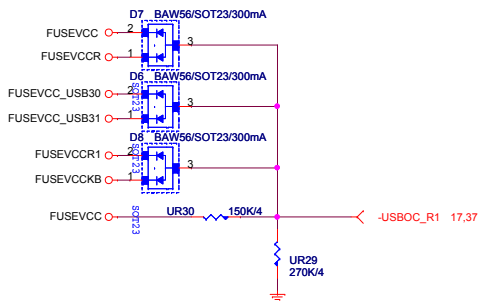
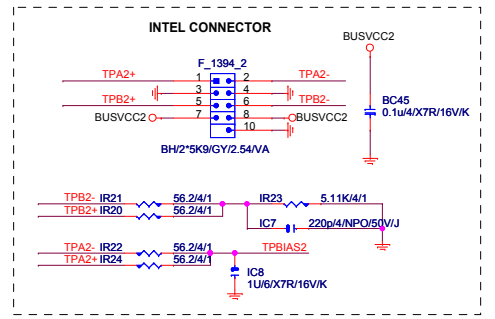
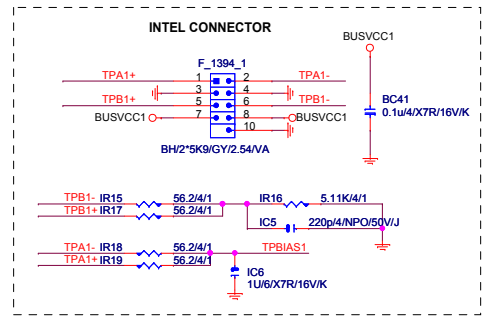
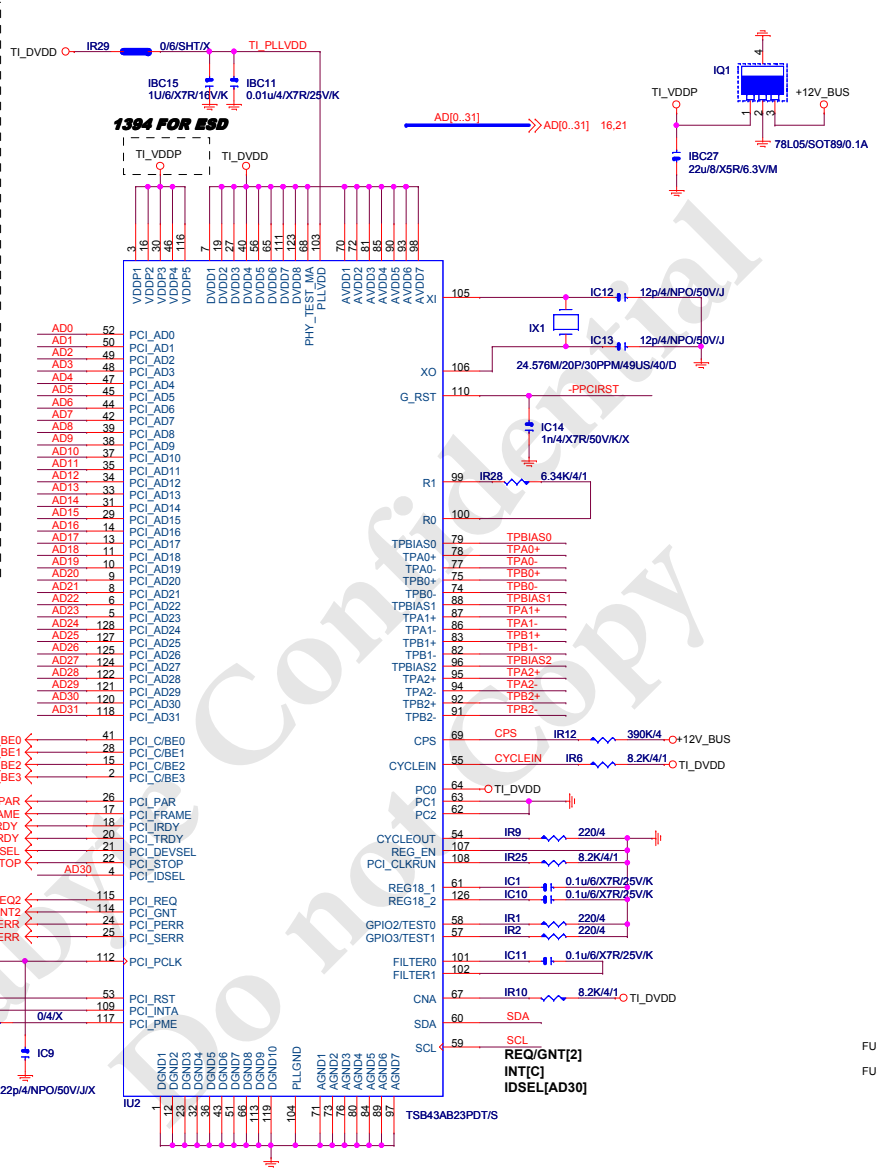
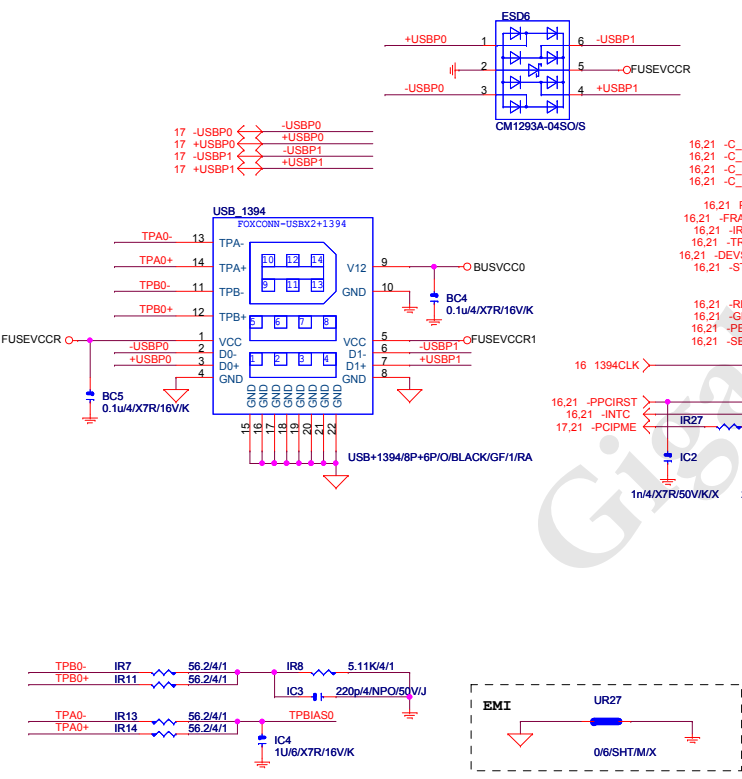
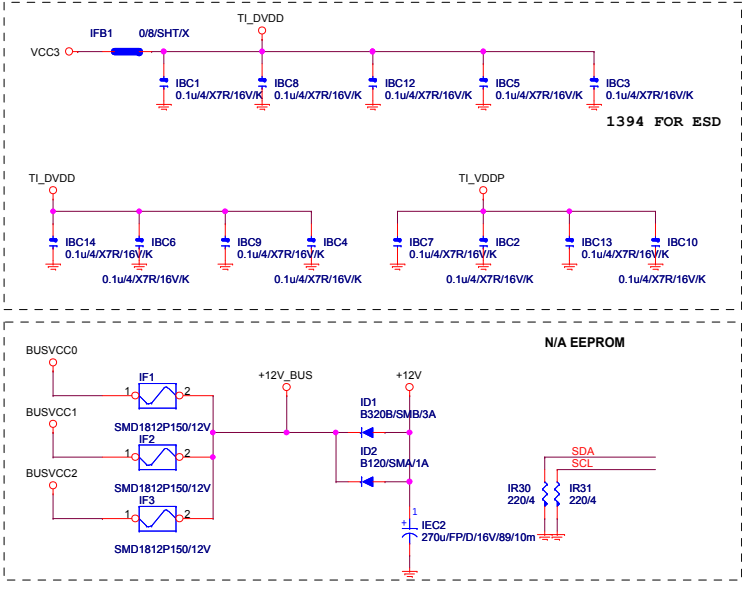
4 VIA to GND

4 VIA to GND

4 VIA to GND

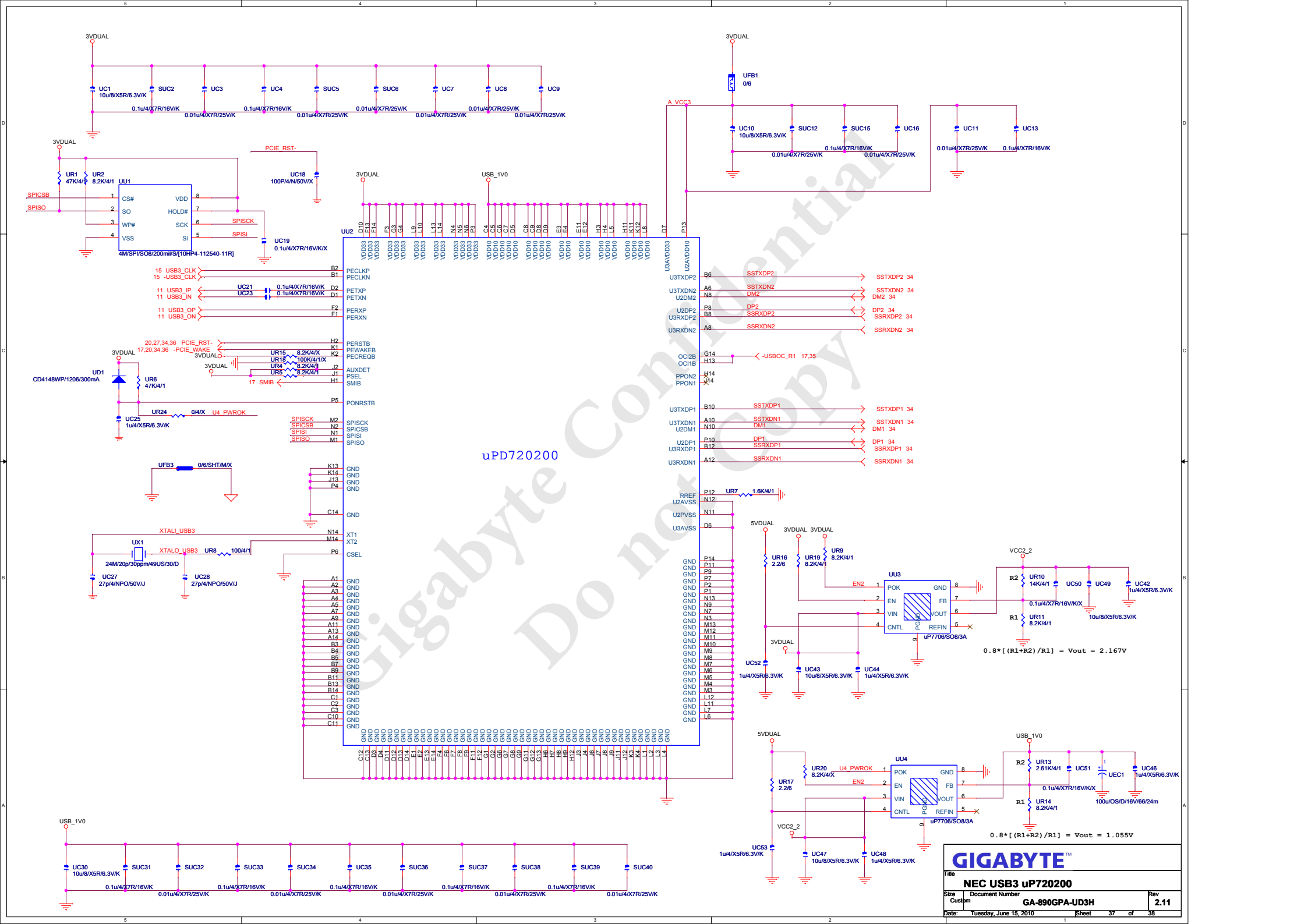
4 VIA to GND











### 3.3V to 1.8V Voltage Regulator

